8 Grid-Imposed Frequency VSC System: Control in *dq*-Frame

8.1 INTRODUCTION

Chapter 5 presented dynamic models for the two-level VSC in $\alpha\beta$-frame and *dq*-frame and briefly discussed its control based on generic block diagrams of Figures 5.5 and 5.7. Chapter 6 introduced the three-level NPC as an extension of the two-level VSC and established that the dynamic model of the three-level NPC is identical to that of the two-level VSC, except that the three-level NPC requires a DC-side voltage equalizing system to maintain DC-side capacitor voltages, each at half the net DC-side voltage. Thus, Chapter 6 presented a unified model for the three-level NPC and the two-level VSC (Fig. 6.18 and 6.19). Chapter 7 introduced a class of VSC systems referred to as *grid-imposed frequency VSC systems*. On the basis of the unified model of Chapter 6, Chapter 7 presented $\alpha\beta$-frame models and controls for two members of the family of the grid-imposed frequency VSC systems, namely, the *real-/reactive-power controller* and the *controlled DC-voltage power port*. In parallel with Chapter 7, this chapter presents *dq*-frame models and controls for the real-/reactive-power controller and the controlled DC-voltage power port.

As discussed in Chapter 7, compared to the *abc*-frame control, the $\alpha\beta$-frame control of a grid-imposed frequency VSC system reduces the number of plants to be controlled from three to two. Moreover, instantaneous decoupled control of the real and reactive power, exchanged between the VSC system and the AC system, is possible in $\alpha\beta$-frame. However, the control variables, that is, feedback signals, feed-forward signals, and control signals are sinusoidal functions of time. It is shown in this chapter that the *dq*-frame control of a grid-imposed VSC system features all merits of the $\alpha\beta$-frame control, in addition to the advantage that the control variables are DC quantities in the steady state. This feature it remarkably facilitates the compensator design, especially in variable-frequency scenarios.

To achieve zero steady-state error in the $\alpha\beta$-frame control, the bandwidth of the closed-loop system must be adequately larger than the AC system frequency; alternatively, the compensators can include complex-conjugate pairs of poles at the AC system frequency and other frequencies of interest, to increase the loop gain. In the *dq*-frame control, however, zero steady-state error is readily achieved by including

Voltage-Sourced Converters in Power Systems, by Amirnaser Yazdani and Reza Iravani

integral terms in the compensators since the control variables are DC quantities [77]. The *dq*-frame representation and control of a grid-imposed VSC system is also consistent with the approach used for the dynamic analysis of the large power system. The small-signal dynamics of the power system is conventionally modeled and analyzed in *dq*-frame [42].

Compared to the $\alpha\beta$-frame control, the *dq*-frame control requires a synchronization mechanism that is usually achieved through the *phase-locked loop* (PLL); this requirement can be regarded a demerit of the *dq*-frame control.

8.2 STRUCTURE OF GRID-IMPOSED FREQUENCY VSC SYSTEM

Figure 8.1 shows a schematic diagram of a grid-imposed frequency VSC system. The VSC represents either a three-level NPC with a DC-side voltage equalizing scheme or a two-level VSC. In either case, the VSC is modeled by a lossless power processor including an equivalent DC-bus capacitor, a current source representing the VSC switching power loss, and series on-state resistances at the AC side representing the VSC conduction power loss, as Figure 8.1 shows. The DC side of the VSC may be interfaced with a DC voltage source or a DC power source. Each phase of the VSC is interfaced with the AC system via a series *RL* branch.

In this chapter, as an approximation we consider an infinitely stiff AC system. Thus, the AC system is modeled by an ideal three-phase voltage source, V_{sabc}.[1] It is also assumed that V_{sabc} is balanced, sinusoidal, and of a relatively constant frequency. The VSC system of Figure 8.1 exchanges the real- and reactive-power components

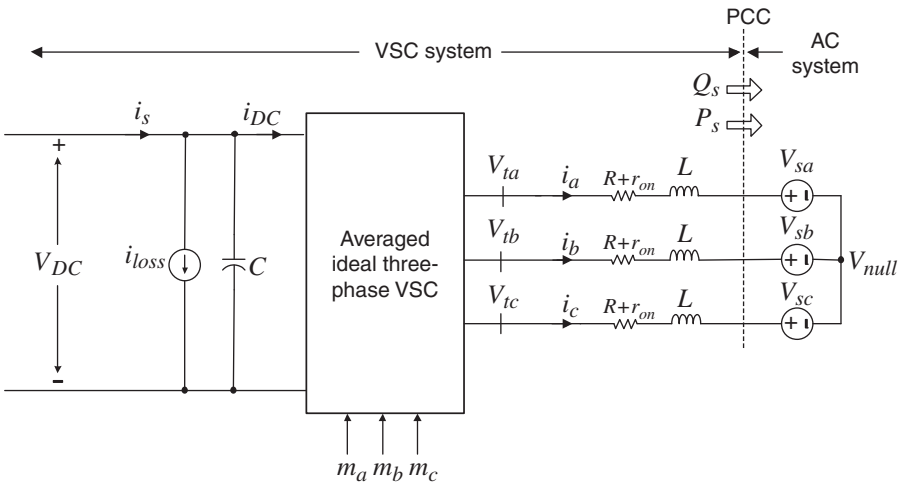

FIGURE 8.1 Schematic diagram of a grid-imposed frequency VSC system.

[1] In Chapter 11, we investigate the dynamics of a VSC system under nonstiff AC system conditions.

$P_s(t)$ and $Q_s(t)$ with the AC system, at the point of common coupling (PCC). Depending on the control strategy, the VSC system of Figure 8.1 is used as either a real-/reactive-power controller or a controlled DC-voltage power port. In Chapter 12, we employ the real-/reactive-power controller as part of a back-to-back HVDC converter system. The controlled DC-voltage power port is employed as part of the static compensator (STATCOM), the back-to-back HVDC converter system, and variable-speed wind-power units, in Chapters 11, 12, and 13, respectively.

8.3 REAL-/REACTIVE-POWER CONTROLLER

The grid-imposed frequency VSC system of Figure 8.1 can be employed as a real-/reactive-power controller. As such, the VSC DC side is connected in parallel with a DC voltage source and the objective is to control the instantaneous real and reactive power that the VSC system exchanges with the AC system, that is, $P_s(t)$ and $Q_s(t)$.

8.3.1 Current-Mode Versus Voltage-Mode Control

Two main methods exist for controlling P_s and Q_s in the VSC system of Figure 8.1. The first approach that is known as *voltage-mode control* and illustrated in Figure 8.2 has been dominantly utilized in high-voltage/-power applications such as in FACTS controllers [44, 45], although its industrial applications have also been reported [47]. Figure 8.2 illustrates that in a voltage-controlled VSC system, the real and reactive

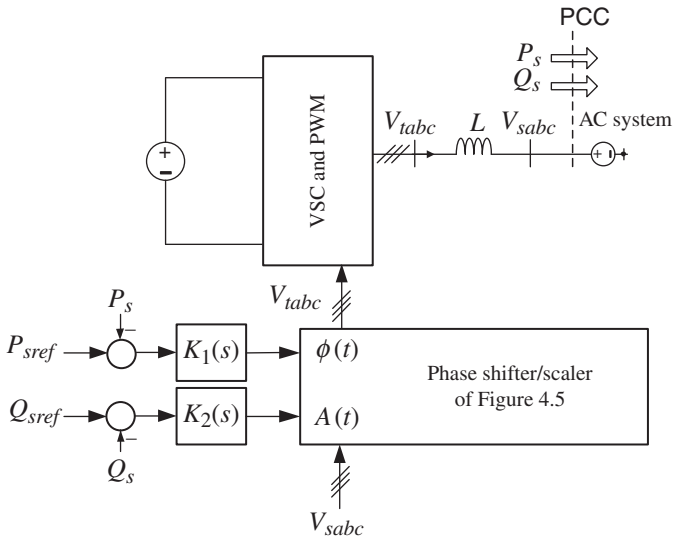

FIGURE 8.2 Schematic diagram of a voltage-controlled real-/reactive-power controller.

power are controlled, respectively, by the phase angle and the amplitude of the VSC AC-side terminal voltage relative to the PCC voltage [46]. If the amplitude and phase angle of V_{tabc} are close to those of V_{sabc}, the real and reactive power are almost decoupled and two independent compensators can be employed for their control (Fig. 8.2). The voltage-mode control is simple and has a low number of control loops. However, the main shortcoming of the voltage-mode control is that there is no control loop closed on the VSC line current. Consequently, the VSC is not protected against overcurrents, and the current may undergo large excursions if the power commands are rapidly changed or faults take place in the AC system.

The second approach to the control of the real and reactive power in the VSC system of Figure 8.1 is referred to as the *current-mode control*. In this approach, the VSC line current is tightly regulated by a dedicated current-control scheme, through the VSC AC-side terminal voltage. Then, the real and reactive power are controlled by the phase angle and the amplitude of the VSC line current with respect to the PCC voltage. Thus, due to the current regulation scheme, the VSC is protected against overcurrent conditions. Other advantages of the current-mode control include robustness against variations in parameters of the VSC system and the AC system, superior dynamic performance, and higher control precision [68]. We demonstrated the basics of the current-mode control strategy in Chapter 3 and will exclusively focus on this method throughout the rest of the book.

Figure 8.3 shows a schematic diagram of a current-controlled real-/reactive-power controller, illustrating that the control is performed in *dq*-frame. Thus, P_s and Q_s are

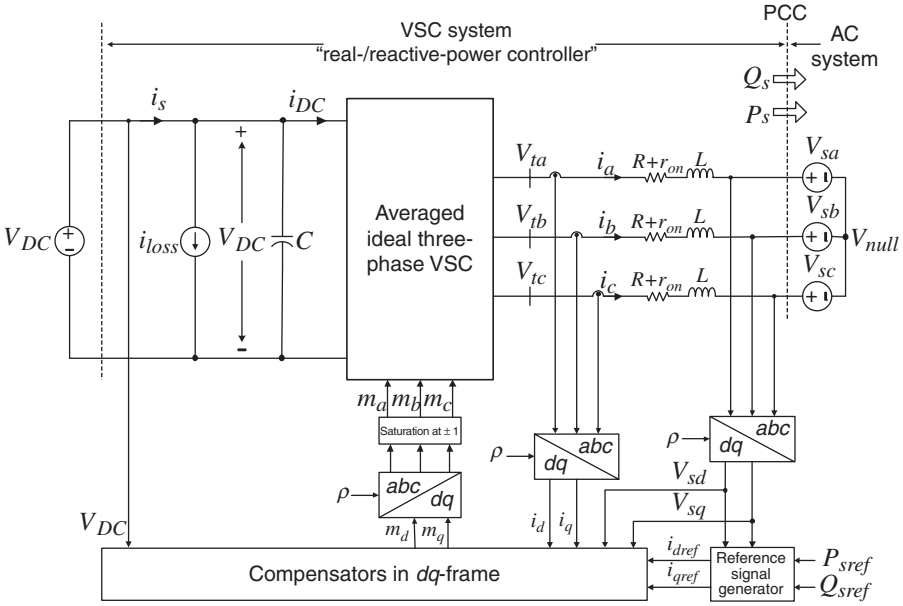

FIGURE 8.3 Schematic diagram of a current-controlled real-/reactive-power controller in *dq*-frame.

controlled by the line current components i_d and i_q. The feedback and feed-forward signals are first transformed to the *dq*-frame and then processed by compensators to produce the control signals in *dq*-frame. Finally, the control signals are transformed to the *abc*-frame and fed to the VSC (Fig. 8.3). To protect the VSC, the reference commands i_{dref} and i_{qref} are limited by the corresponding saturation blocks (not shown in the figure). It is noted that the block diagram of Figure 8.3 is a special case of the general block diagram of Figure 4.27. In Chapter 12, we employ the real-/reactive-power controller as part of the back-to-back HVDC converter system.

8.3.2 Representation of Space Phasors in *dq*-Frame

In this chapter, we need to express space phasors in *dq*-frame. The transformation and its inverse were extensively discussed in Chapter 4. However, they are briefly reviewed in this section, for ease of reference.

Consider the space phasor $\overrightarrow{f}(t) = f_\alpha + jf_\beta$. The *dq*- to $\alpha\beta$-frame transformation is defined as

$$f_d + jf_q = \overrightarrow{f}(t)e^{-j\rho(t)} = (f_\alpha + jf_\beta)e^{-j\rho(t)}, \tag{8.1}$$

which is a phase shift in $\overrightarrow{f}(t)$ by $-\rho(t)$. The angle $\rho(t)$ can be chosen arbitrarily. However, if, for example, $\overrightarrow{f}(t) = \widehat{f}e^{j(\omega t+\theta_0)}$, then choosing $\rho(t)$ to be equal to ωt results in the space phasor

$$f_d + jf_q = \underbrace{\widehat{f}e^{j(\omega t+\theta_0)}}_{\overrightarrow{f}(t)} e^{-j\omega t} = \widehat{f}e^{j\theta_0},$$

which is no longer time-varying and, therefore, f_d and f_q are DC quantities. The inverse transformation is

$$\overrightarrow{f}(t) = f_\alpha + jf_\beta = (f_d + jf_q)e^{j\rho(t)}. \tag{8.2}$$

8.3.3 Dynamic Model of Real-/Reactive-Power Controller

Assume that the AC system voltage in the VSC system of Figure 8.3 is expressed as

$$\begin{aligned}
V_{sa}(t) &= \widehat{V}_s \cos(\omega_0 t + \theta_0), \\
V_{sb}(t) &= \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right), \\
V_{sc}(t) &= \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right),
\end{aligned} \tag{8.3}$$

where $\widehat{V}_s$ is the peak value of the line-to-neutral voltage, ω_0 is the AC system (source) frequency, and θ_0 is the source initial phase angle. Based on (4.2), the space-phasor equivalent of V_{s-abc} is

$$\overrightarrow{V_s}(t) = \widehat{V}_s e^{j(\omega_0 t+\theta_0)}. \tag{8.4}$$

Dynamics of the AC side of the VSC system of Figure 8.3 are described by the following space-phasor equation (refer to (7.11) for details):

$$L\frac{d\overrightarrow{i}}{dt} = -(R + r_{on})\overrightarrow{i} + \overrightarrow{V_t} - \overrightarrow{V_s}. \tag{8.5}$$

Substituting for $\overrightarrow{V_s}$ from (8.4) in (8.5), we deduce

$$L\frac{d\overrightarrow{i}}{dt} = -(R + r_{on})\overrightarrow{i} + \overrightarrow{V_t} - \widehat{V}_s e^{j(\omega_0 t+\theta_0)}. \tag{8.6}$$

Then, we use (8.2) to express (8.6) in a dq-frame. Thus, substituting for $\overrightarrow{i} = i_{dq}e^{j\rho}$ and $\overrightarrow{V_t} = V_{tdq}e^{j\rho}$ in (8.6), we deduce

$$L\frac{d}{dt}\left(i_{dq}e^{j\rho}\right) = -(R + r_{on})\left(i_{dq}e^{j\rho}\right) + \left(V_{tdq}e^{j\rho}\right) - \widehat{V}_s e^{j(\omega_0 t+\theta_0)}, \tag{8.7}$$

where $f_{dq} = f_d + jf_q$. Equation (8.7) can be rewritten as

$$L\frac{d}{dt}\left(i_{dq}\right) = -j\left(L\frac{d\rho}{dt}\right)i_{dq} - (R + r_{on})i_{dq} + V_{tdq} - \widehat{V}_s e^{j(\omega_0 t+\theta_0-\rho)}. \tag{8.8}$$

Decomposing (8.8) into real and imaginary components, we deduce

$$L\frac{di_d}{dt} = \left(L\frac{d\rho}{dt}\right)i_q - (R + r_{on})\,i_d + V_{td} - \widehat{V}_s\cos(\omega_0 t + \theta_0 - \rho), \tag{8.9}$$

$$L\frac{di_q}{dt} = -\left(L\frac{d\rho}{dt}\right)i_d - (R + r_{on})\,i_q + V_{tq} - \widehat{V}_s\sin(\omega_0 t + \theta_0 - \rho). \tag{8.10}$$

Equations (8.9) and (8.10) are not in the standard state-space form. Thus, we introduce the new control variable ω to (8.9) and (8.10), where $\omega = d\rho/dt$. This yields

$$L\frac{di_d}{dt} = L\omega(t)i_q - (R + r_{on})i_d + V_{td} - \widehat{V}_s \cos(\omega_0 t + \theta_0 - \rho), \tag{8.11}$$

$$L\frac{di_q}{dt} = -L\omega(t)i_d - (R + r_{on})i_q + V_{tq} - \widehat{V}_s \sin(\omega_0 t + \theta_0 - \rho), \tag{8.12}$$

$$\frac{d\rho}{dt} = \omega(t). \tag{8.13}$$

In (8.11)–(8.13), i_d, i_q, and ρ are the state variables, and V_{td}, V_{tq}, and ω are the control inputs. The system described by (8.11)–(8.13) is nonlinear due to the presence of the terms ωi_d, ωi_q, $\cos(\omega_0 t + \theta_0 - \rho)$, and $\sin(\omega_0 t + \theta_0 - \rho)$.

To further investigate (8.11)–(8.13), assume that ρ has a zero initial condition and $\omega(t) \equiv 0$. Consequently, ρ remains zero at all times, and (8.11) and (8.12) assume the forms

$$L\frac{di_d}{dt} = -(R + r_{on})i_d + V_{td} - \widehat{V}_s \cos(\omega_0 t + \theta_0), \tag{8.14}$$

$$L\frac{di_q}{dt} = -(R + r_{on})i_q + V_{tq} - \widehat{V}_s \sin(\omega_0 t + \theta_0). \tag{8.15}$$

Equations (8.14) and (8.15) describe two, decoupled, first-order systems that are excited by inputs $-\widehat{V}_s \cos(\omega_0 t + \theta_0)$ and $-\widehat{V}_s \sin(\omega_0 t + \theta_0)$, respectively. Thus, the superposition principle requires that i_d and i_q also include sinusoidal components, irrespective of V_{td} and V_{tq}. This result is expected since if $\rho = 0$, then based on (8.1) the dq-frame is the same as the $\alpha\beta$-frame in which the signals are sinusoidal functions of time. In other words, (8.14) and (8.15) represent the VSC system in $\alpha\beta$-frame; comparison of (8.14) and (8.15), respectively, with (7.12) and (7.13) confirms this conclusion.

The foregoing discussion shows that the usefulness of the dq-frame depends on proper selection of ω and ρ. For the VSC system of Figure 8.3, if $\omega = \omega_0$ and $\rho(t) = \omega_0 t + \theta_0$, then (8.11) and (8.12) take the forms

$$L\frac{di_d}{dt} = L\omega_0 i_q - (R + r_{on})i_d + V_{td} - \widehat{V}_s, \tag{8.16}$$

$$L\frac{di_q}{dt} = -L\omega_0 i_d - (R + r_{on})i_q + V_{tq}, \tag{8.17}$$

which describe a second-order linear system that is excited by the constant input $\widehat{V}_s$. Thus, if V_{td} and V_{tq} are DC variables, i_d and i_q are also DC variables in the steady state. The mechanism to ensure $\rho(t) = \omega_0 t + \theta_0$ is referred to as the PLL. The following section presents the structure, model, and stabilization of the PLL.

8.3.4 Phase-Locked Loop (PLL)

Substituting for $\overrightarrow{V_s}(t)$ from (8.4) in (8.1), we deduce

$$V_{sd} = \widehat{V}_s \cos(\omega_0 t + \theta_0 - \rho), \tag{8.18}$$

$$V_{sq} = \widehat{V}_s \sin(\omega_0 t + \theta_0 - \rho). \tag{8.19}$$

Thus, (8.11)–(8.13) can be rewritten as

$$L\frac{di_d}{dt} = L\omega(t)i_q - (R + r_{on})i_d + V_{td} - V_{sd}, \tag{8.20}$$

$$L\frac{di_q}{dt} = -L\omega(t)i_d - (R + r_{on})i_q + V_{tq} - V_{sq}, \tag{8.21}$$

$$\frac{d\rho}{dt} = \omega(t). \tag{8.22}$$

Based on (8.19), $\rho(t) = \omega_0 t + \theta_0$ corresponds to $V_{sq} = 0$. Therefore, we devise a mechanism to regulate V_{sq} at zero. This can be achieved based on the following feedback law:

$$\omega(t) = H(p)V_{sq}(t), \tag{8.23}$$

where $H(p)$ is a linear transfer function (compensator) and $p = d(\cdot)/dt$ is a differentiation operator. Substituting for V_{sq} from (8.19) in (8.23), and substituting for ω from (8.23) in (8.22), we deduce

$$\frac{d\rho}{dt} = H(p)\widehat{V}_s \sin(\omega_0 t + \theta_0 - \rho). \tag{8.24}$$

Equation (8.24) describes a nonlinear dynamic system, which is referred to as PLL [49], [78–80]. The function of the PLL is to regulate ρ at $\omega_0 t + \theta_0$. However, in view of its nonlinear characteristic, the PLL can exhibit unsatisfactory behavior under certain conditions. For example, if the PLL starts from an initial condition corresponding to $\rho(0) = 0$ and $\omega(0) = 0$, then the term $\widehat{V}_s H(p) \sin(\omega_0 t + \theta_0 - \rho)$ in (8.24) is a sinusoidal function of time with frequency ω_0. Then, if $H(s)$ has a low-pass frequency response, the right-hand side of (8.24) and also $d\rho/dt$ exhibit small sinusoidal perturbations about zero, the PLL falls in a limit cycle, and ρ does not track $\omega_0 t + \theta_0$. To prevent the limit cycle from taking place, the control law can be modified as

$$\omega(t) = H(p)V_{sq}(t), \quad \omega(0) = \omega_0 \ \text{ and } \ \omega_{min} \le \omega \le \omega_{max}, \tag{8.25}$$

where $\omega(t)$ has the initial value $\omega(0) = \omega_0$ and is limited to the lower and upper limits of, respectively, ω_{min} and ω_{max}. ω_{min} and ω_{max} are selected to be close to ω_0 and thus to define a narrow range of variations for $\omega(t)$. On the other hand, the range of

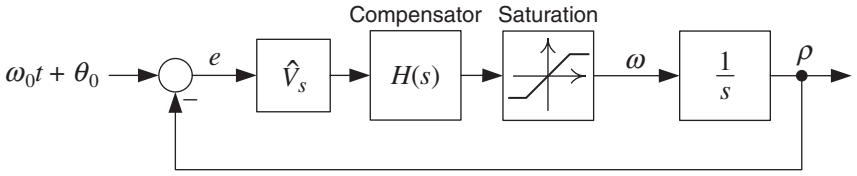

FIGURE 8.4 Control block diagram of the PLL.

variations should be selected adequately wide to permit excursions of $\omega(t)$ during transients. If the PLL tracks $\omega_0 t + \theta_0$, the term $\omega_0 t + \theta_0 - \rho$ is close to zero and $\sin(\omega_0 t + \theta_0 - \rho) \approx (\omega_0 t + \theta_0 - \rho)$. Therefore, (8.24) can be simplified to

$$\frac{d\rho}{dt} = \widehat{V}_s H(p)(\omega_0 t + \theta_0 - \rho). \tag{8.26}$$

Equation (8.26) represents a classical feedback control loop in which $\omega_0 t + \theta_0$ is the reference input, ρ is the output, and $\widehat{V}_s H(s)$ is the transfer function of the effective compensator, as shown in the block diagram of Figure 8.4.

Figure 8.5 illustrates a schematic diagram of the PLL based on (8.19), (8.22), and (8.23). Figure 8.5 shows that the PLL transforms V_{sabc} to V_{sdq} (based on (4.73)) and adjusts the rotational speed of the *dq*-frame, that is, ω, such that V_{sq} is forced to zero in the steady state. The end result is that $\rho = \omega_0 t + \theta_0$ and $V_{sd} = \widehat{V}_s$. It should be pointed out that in the block diagram of Figure 8.5, the integrator of (8.22) is realized by means of a voltage-controlled oscillator (VCO). The VCO can be regarded as a resettable integrator whose output, ρ, is reset to zero whenever it reaches 2π.

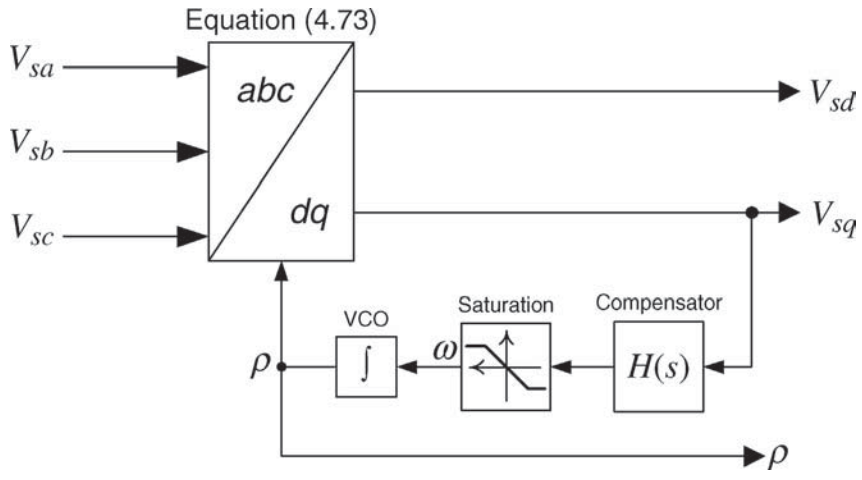

FIGURE 8.5 Schematic diagram of the PLL.

8.3.5 Compensator Design for PLL

Dynamic performance of the PLL is highly influenced by the compensator $H(s)$. Consider the block diagram of Figure 8.4 indicating that the reference signal, $\omega_0 t + \theta_0$, is composed of a constant component, that is, θ_0, and a ramp function, that is, $\omega_0 t$. Since the loop gain includes an integral term, ρ tracks the constant component of the reference signal with zero steady-state error. However, to ensure a zero steady-state error for the ramp component, the loop gain must include at least two integrators. Therefore, $H(s)$ must include at least one integral term, that is, one pole at $s = 0$. The other poles and zeros of $H(s)$ are determined mainly on the basis of the closed-loop bandwidth of the PLL and stability indices such as phase margin and gain margin.

Another consideration in designing $H(s)$ is the issue of unbalanced and/or harmonically distorted three-phase voltages. Assume that V_{sabc} represents an unbalanced voltage with a negative-sequence fundamental component and a fifth-order harmonic component [81], as

$$\begin{aligned}
V_{sa}(t) &= \widehat{V}_s \cos(\omega_0 t + \theta_0) + k_1 \widehat{V}_s \cos(\omega_0 t + \theta_0) \\
&\quad + k_5 \widehat{V}_s \cos(5\omega_0 t + \phi_5), \\
V_{sb}(t) &= \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) + k_1 \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) \\
&\quad + k_5 \widehat{V}_s \cos\left(5\omega_0 t + \phi_5 - \frac{4\pi}{3}\right), \\
V_{sc}(t) &= \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) + k_1 \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) \\
&\quad + k_5 \widehat{V}_s \cos\left(5\omega_0 t + \phi_5 - \frac{2\pi}{3}\right),
\end{aligned} \tag{8.27}$$

where k_1 and k_5 are the amplitudes of the negative-sequence (fundamental) and fifth-order harmonic components, respectively, relative to the amplitude of the positive-sequence (fundamental) component. Based on (4.2), the space phasor corresponding to V_{sabc} is

$$\overrightarrow{V_s} = \widehat{V}_s e^{j(\omega_0 t + \theta_0)} + k_1 \widehat{V}_s e^{-j(\omega_0 t + \theta_0)} + k_5 \widehat{V}_s e^{-j(5\omega_0 t + \phi_5)}. \tag{8.28}$$

If the PLL of Figure 8.5 is under a steady-state operating condition, that is, $\rho = \omega_0 t + \theta_0$, then based on (8.1) V_{sd} and V_{sq} are

$$V_{sd} = \widehat{V}_s + k_1 \widehat{V}_s \cos(2\omega_0 t + 2\theta_0) + k_5 \widehat{V}_s \cos(6\omega_0 t + \theta_0 + \phi_5), \tag{8.29}$$

$$V_{sq} = -k_1 \widehat{V}_s \sin(2\omega_0 t + 2\theta_0) - k_5 \widehat{V}_s \sin(6\omega_0 t + \theta_0 + \phi_5). \tag{8.30}$$

Equations (8.29) and (8.30) indicate that, in addition to DC components, V_{sd} and V_{sq} include sinusoidal components with frequencies $2\omega_0$ and $6\omega_0$. Typical values

of k_1 and k_5 are assumed to be 0.01 and 0.025, respectively [81]. However, under single-phase to ground faults, k_1 can be as large as 0.5. The sinusoidal components of V_{sq} must be attenuated by $H(s)$. Otherwise, ω and ρ also exhibit fluctuations that are modulated with feedback and control signals, through *abc*- to *dq*-frame and *dq*- to *abc*-frame transformations, and result in generation of undesirable voltage/current distortions in the VSC system.

Between the two AC components of V_{sq}, the component with frequency $2\omega_0$ is more important. The reason is that (i) the frequency of this component is three times lower than that of the other component and (ii) the magnitude of this component, k_1, can be significantly larger than that of the other component, for example, during a fault. One approach to attenuate the double-frequency component of V_{sq} is to ensure that $H(s)$ exhibits a strong low-pass characteristic. However, this method may compromise the PLL closed-loop bandwidth. Alternatively, one can include in $H(s)$ one pair of complex-conjugate zeros, at $s = \pm j2\omega_0$, to eliminate the double-frequency ripple of V_{sq}. The advantage of this technique is that the PLL closed-loop bandwidth is not sacrificed and can be selected to be arbitrarily large. Example 8.1 illustrates the second PLL design approach.

EXAMPLE 8.1 Compensator Design for the PLL

Consider the PLL of Figure 8.5 whose input is V_{sabc} defined by (8.27), where $\omega_0 = 2\pi \times 60$ rad/s and $\widehat{V}_s = 391$ V. The objective is to design the PLL compensator $H(s)$.

As explained in Section 8.3.5, $H(s)$ must include one pole at $s = 0$ and the complex-conjugate zeros $s = \pm j2\omega_0$. In addition, to ensure that the loop gain magnitude continues to drop with the slope of -40 dB/dec for $\omega > 2\omega_0$, a double real pole at $s = -2\omega_0$ is included in $H(s)$. Thus,

$$H(s) = \left(\frac{h}{\widehat{V}_{sn}}\right) \frac{s^2 + (2\omega_0)^2}{s\,(s + 2\omega_0)^2} F(s), \tag{8.31}$$

where $\widehat{V}_{sn}$ is the nominal value of $\widehat{V}_s$ and $F(s)$ is the proper transfer function with no zero at $s = 0$. Based on the block diagram of Figure 8.4, the loop gain is formulated as

$$\ell(s) = h \frac{s^2 + (2\omega_0)^2}{s^2(s + 2\omega_0)^2} F(s). \tag{8.32}$$

Let us assume that we need a gain crossover frequency of $\omega_c = 200$ rad/s and a phase margin of 60°. If $hF(s) = 1$, it can be calculated that $\angle \ell(j200) = -210^\circ$. Thus, to achieve the required phase margin, $F(j200)$ must add 90° to $\angle \ell(j200)$. As discussed in Example 3.6, a lead compensator can offer an optimum phase advance to the loop gain. In this example, the required phase advance is fairly large. Consequently, $F(s)$ can be composed of two cascaded lead compensators,

each to provide 45° at 200 rad/s. Thus,

$$F(s) = \left(\frac{s + (p/\alpha)}{s + p}\right)\left(\frac{s + (p/\alpha)}{s + p}\right), \tag{8.33}$$

where

$$p = \omega_c\sqrt{\alpha} \tag{8.34}$$

$$\alpha = \frac{1 + \sin\delta_m}{1 - \sin\delta_m}, \tag{8.35}$$

and δ_m is the phase of each lead compensator at ω_c. If $\delta_m = 45°$, based on (8.33)–(8.35), we calculate $F(s)$ as

$$F(s) = \left(\frac{s + 83}{s + 482}\right)^2. \tag{8.36}$$

Substituting for $F(s)$ from (8.36) in (8.32), we deduce

$$\ell(s) = \frac{h\left(s^2 + 568{,}516\right)\left(s^2 + 166s + 6889\right)}{s^2\left(s^2 + 1508s + 568{,}516\right)\left(s^2 + 964s + 232{,}324\right)}. \tag{8.37}$$

It then follows from $|\ell(j200)| = 1$ and $\widehat{V}_{sn} = 391$ V that $h = 2.68 \times 10^5$. Therefore, $h/\widehat{V}_{sn} = 685.42$ and the final compensator is

$$H(s) = \frac{685.42\left(s^2 + 568{,}516\right)\left(s^2 + 166s + 6889\right)}{s\left(s^2 + 1508s + 568{,}516\right)\left(s^2 + 964s + 232{,}324\right)} \quad [(\text{rad/s})/\text{V}]. \tag{8.38}$$

Figure 8.6 depicts the frequency response of $\ell(j\omega)$ based on the compensator of (8.38). It is observed that $|\ell(j\omega)|$ drops with the slope of −40 dB/dec, for $\omega \ll \omega_c = 200$. However, around ω_c the slope of $|\ell(j\omega)|$ reduces to about −20 dB/dec and $\angle\ell(j\omega)$ rises to about −120° at $\omega = \omega_c$, corresponding to a phase margin of 60°. Figure 8.6 also illustrates that $|\ell(j\omega)|$ continues to drop with a slope of −40 dB/dec for $\omega > \omega_c$. This characteristic is desired as the AC components of V_{sq} due to the harmonic distortion of V_{sabc} are attenuated. In particular, at $\omega = 6\omega_0$, $|\ell(j\omega)|$ is about −30 dB.

Figure 8.7 illustrates the start-up transient of the PLL. Figure 8.7 shows that, from $t = 0$ to $t = 0.07$ s, the compensator output is saturated at $\omega_{min} = 2\pi \times 55$ rad/s and, therefore, V_{sd} and V_{sq} vary with time. At about $t = 0.07$ s, V_{sq} crosses zero and intends to become negative. Thus, $H(s)$ increases ω to regulate V_{sq} at zero. Figure 8.7 indicates that V_{sq} is regulated at zero within 0.15 s. It should be noted that if ω_{min} is selected closer to ω_0, the start-up transient period becomes shorter. However, ω_{min} cannot be selected too close to ω_0 since the PLL would not be able to quickly react to other types of disturbance.

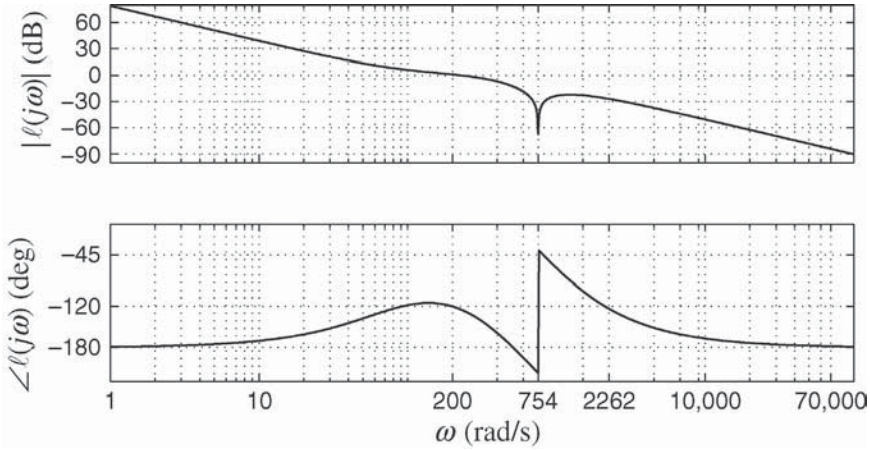

FIGURE 8.6 Open-loop frequency response of the PLL of Example 8.1.

Figure 8.8 illustrates the dynamic response of the PLL to a sudden imbalance in V_{sabc}. Initially, the PLL is in a steady state. At $t = 0.05$ s, the AC system voltage V_{sabc} becomes unbalanced such that $\widehat{V}_s$ and k_1 undergo step changes, respectively, from 391 to 260 V and from zero to 0.5, and at $t = 0.15$ s, V_{sabc}

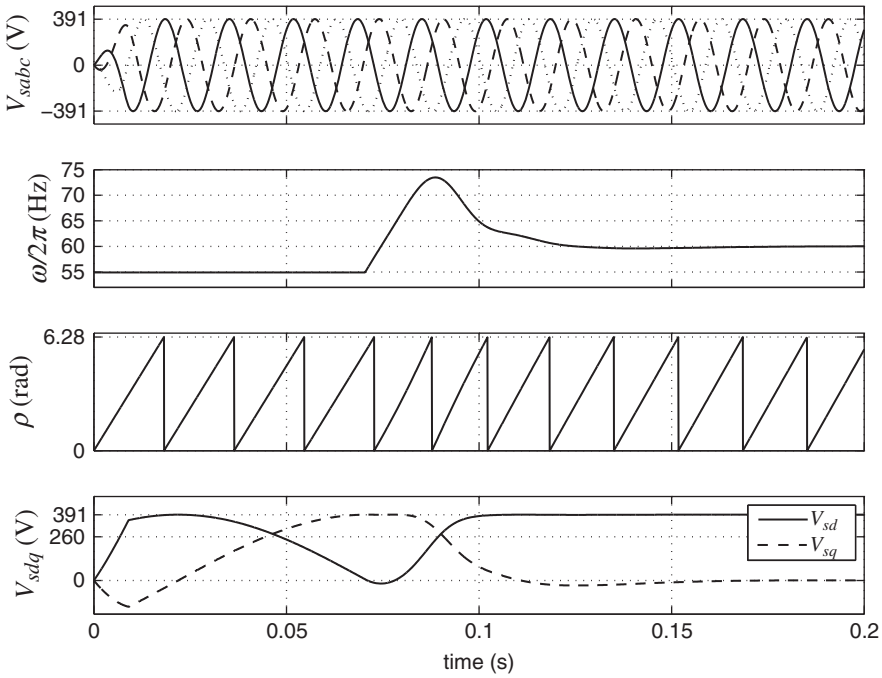

FIGURE 8.7 Start-up response of the PLL of Example 8.1.

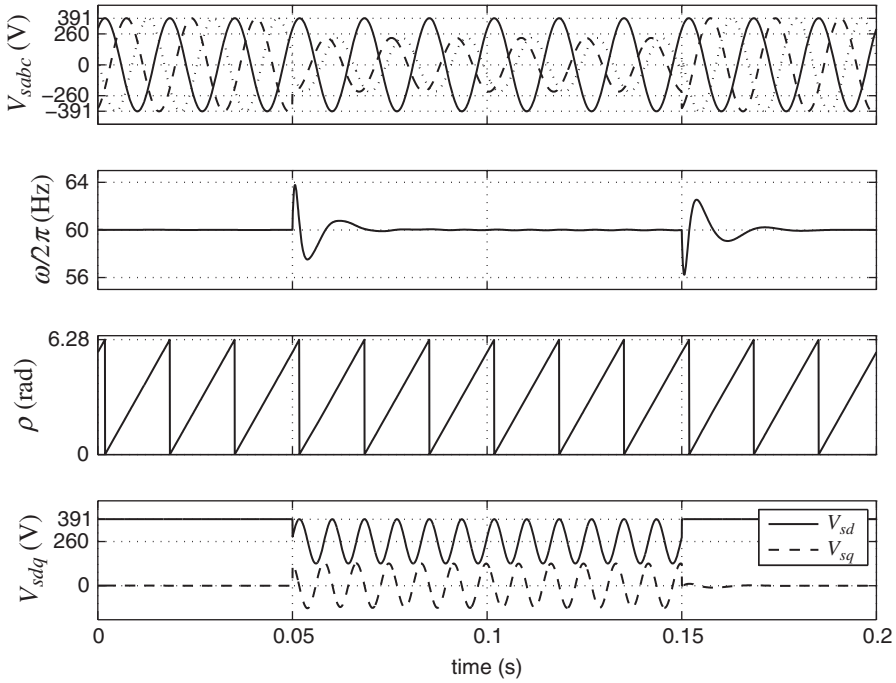

FIGURE 8.8 Response of the PLL of Example 8.1 to a sudden AC system voltage imbalance.

reverts to its balanced predisturbance condition. In response to the voltage imbalance, $H(s)$ transiently changes ω, as Figure 8.8 shows, to maintain the DC component of V_{sq} at zero. Figure 8.8 also shows that V_{sq} (and V_{sd}) includes a 120-Hz sinusoidal ripple due to the negative-sequence component of V_{sabc}. The ripple is, however, suppressed by $H(s)$, and ω and ρ remain free of distortion.

Figure 8.9 depicts the dynamic response of the PLL to two stepwise changes in ω_0, the first one from $2\pi \times 60 = 377$ rad/s to $2\pi \times 63 = 396$ rad/s at $t = 0.05$ s, and the other from 396 rad/s to $2\pi \times 57 = 358$ rad/s at $t = 0.1$ s. As Figure 8.9 shows, V_{sq} is rapidly regulated at zero and ω tracks the changes.

Equation (8.31) denotes that $H(s)$ is normalized such that the constant gain of the loop gain h is independent of $\widehat{V}_{sn}$. Thus, in subsequent chapters when we need a PLL, we will employ the compensator of (8.38), but modify its constant gain, that is, $h/\widehat{V}_{sn}$, according to $\widehat{V}_{sn}$ for the specific problem in hand, based on $h = 2.68 \times 10^5$.

8.4 CURRENT-MODE CONTROL OF REAL-/REACTIVE-POWER CONTROLLER

With reference to the real-/reactive-power controller of Figure 8.3, based on (4.83) and (4.84), the real and reactive power delivered to the AC system at

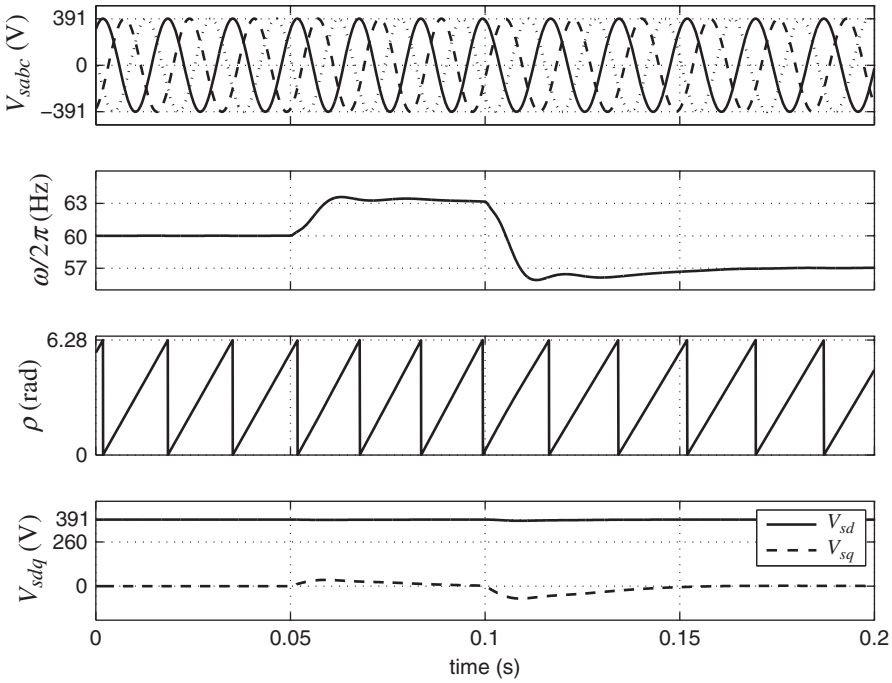

FIGURE 8.9 Response of the PLL of Example 8.1 to a sudden AC system frequency change.

the PCC are

$$P_s(t) = \frac{3}{2}\left[V_{sd}(t)i_d(t) + V_{sq}(t)i_q(t)\right], \tag{8.39}$$

$$Q_s(t) = \frac{3}{2}\left[-V_{sd}(t)i_q(t) + V_{sq}(t)i_d(t)\right], \tag{8.40}$$

where V_{sd} and V_{sq} are the AC system dq-frame voltage components and cannot be controlled by the VSC system. As described in Section 8.3.4, if the PLL is in a steady state, $V_{sq} = 0$ and (8.39) and (8.40) can be rewritten as

$$P_s(t) = \frac{3}{2}V_{sd}(t)i_d(t), \tag{8.41}$$

$$Q_s(t) = -\frac{3}{2}V_{sd}(t)i_q(t). \tag{8.42}$$

Therefore, based on (8.41) and (8.42), $P_s(s)$ and $Q_s(s)$ can be controlled by i_d and i_q, respectively. Let us introduce

$$i_{dref}(t) = \frac{2}{3V_{sd}} P_{sref}(t), \tag{8.43}$$

$$i_{qref}(t) = -\frac{2}{3V_{sd}} Q_{sref}(t). \tag{8.44}$$

Then, if the control system can provide fast reference tracking, that is, $i_d \approx i_{dref}$ and $i_q \approx i_{qref}$, then $P_s \approx P_{sref}$ and $Q_s \approx Q_{sref}$, that is, $P_s(t)$ and $Q_s(t)$, can be independently controlled by their respective reference commands. Since V_{sd} is a DC variable (in the steady state), i_{dref} and i_{qref} are also DC variables if P_{sref} and Q_{sref} are constant signals. Thus, as expected, the control system in dq-frame deals with DC variables, unlike the control system in $\alpha\beta$-frame that deals with sinusoidal signals.

8.4.1 VSC Current Control

The dq-frame control of the real-/reactive-power controller of Figure 8.3 is based on (8.11) and (8.12). Assuming a steady-state operating condition and substituting for $\omega(t) = \omega_0$ in (8.11) and (8.12), we deduce

$$L\frac{di_d}{dt} = L\omega_0 i_q - (R + r_{on})i_d + V_{td} - V_{sd}, \tag{8.45}$$

$$L\frac{di_q}{dt} = -L\omega_0 i_d - (R + r_{on})i_q + V_{tq} - V_{sq}, \tag{8.46}$$

in which, based on (5.22) and (5.23), V_{td} and V_{tq} are

$$V_{td}(t) = \frac{V_{DC}}{2} m_d(t), \tag{8.47}$$

$$V_{tq}(t) = \frac{V_{DC}}{2} m_q(t). \tag{8.48}$$

Equations (8.47) and (8.48) represent the VSC model in dq-frame. The model is applicable to both the two-level VSC and the three-level NPC. In (8.45) and (8.46), i_d and i_q are state variables, V_{td} and V_{tq} are control inputs, and V_{sd} and V_{sq} are disturbance inputs. Due to the presence of $L\omega_0$ terms in (8.45) and (8.46), dynamics of i_d and i_q are coupled. To decouple the dynamics, we determine m_d and m_q as

$$m_d = \frac{2}{V_{DC}} \big(u_d - L\omega_0 i_q + V_{sd}\big), \tag{8.49}$$

$$m_q = \frac{2}{V_{DC}} \big(u_q + L\omega_0 i_d + V_{sq}\big), \tag{8.50}$$

where u_d and u_q are two new control inputs [69, 82]. Substituting for m_d and m_q in (8.47) and (8.48), respectively, from (8.49) and (8.50), and substituting for V_{td} and

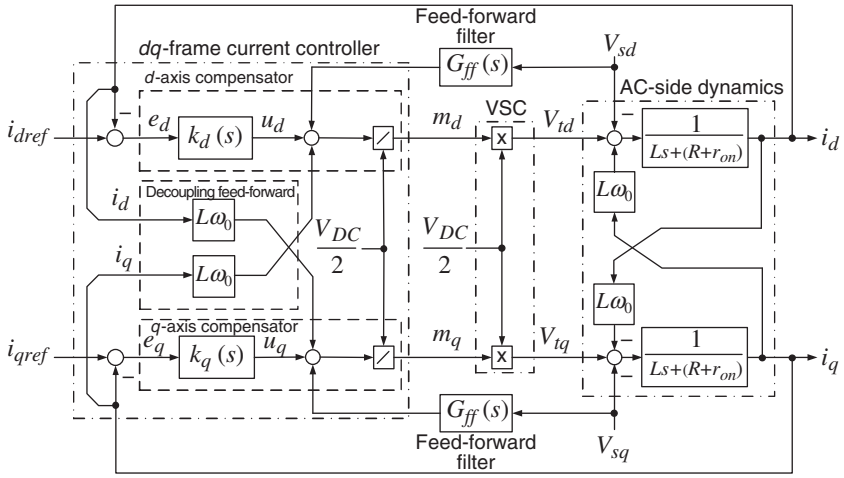

FIGURE 8.10 Control block diagram of a current-controlled VSC system.

V_{tq} from the resultant in (8.45) and (8.46), we deduce

$$L\frac{di_d}{dt} = -(R + r_{on})i_d + u_d, \tag{8.51}$$

$$L\frac{di_q}{dt} = -(R + r_{on})i_q + u_q. \tag{8.52}$$

Equations (8.51) and (8.52) describe two decoupled, first-order, linear systems. Based on (8.51) and (8.52), i_d and i_q can be controlled by u_d and u_q, respectively. Figure 8.10 shows a block representation of the d- and q-axis current controllers of the VSC system in which u_d and u_q are the outputs of two corresponding compensators. The d-axis compensator processes $e_d = i_{dref} - i_d$ and provides u_d. Then, based on (8.49), u_d contributes to m_d. Similarly, the q-axis compensator processes $e_q = i_{qref} - i_q$ and provides u_q that, based on (8.50), contributes to m_q. The VSC then amplifies m_d and m_q by a factor of $V_{DC}/2$ and generates V_{td} and V_{tq} that, in turn, control i_d and i_q based on (8.45) and (8.46). On the basis of the above-mentioned control process, one can sketch the simplified control block diagram of Figure 8.11, which is equivalent to the control system of Figure 8.10. It should be noted that in the control system of Figure 8.10, all the control, feed-forward, and feedback signals are DC quantities in the steady state.

Figure 8.11 indicates that the control plants in both d- and q-axis current-control loops are identical. Therefore, the corresponding compensators can also be identical. Consider the d-axis control loop. Unlike the $\alpha\beta$-frame control where the compensators are fairly difficult to optimize and typically are of high dynamic orders, $k_d(s)$ can be a simple proportional-integral (PI) compensator to enable tracking of a DC reference

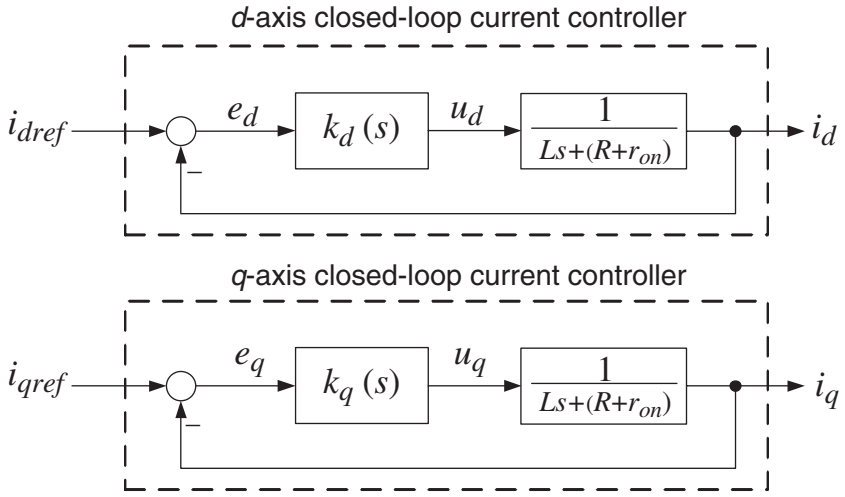

FIGURE 8.11 Simplified block diagram of the current-controlled VSC system of Figure 8.10.

command. Let

$$k_d(s) = \frac{k_p s + k_i}{s}, \tag{8.53}$$

where k_p and k_i are proportional and integral gains, respectively. Thus, the loop gain is

$$\ell(s) = \left(\frac{k_p}{Ls}\right) \frac{s + k_i/k_p}{s + (R + r_{on})/L}. \tag{8.54}$$

It is noted that due to the plant pole at $s = -(R + r_{on})/L$, which is fairly close to the origin, the magnitude and the phase of the loop gain start to drop from a relatively low frequency. Thus, the plant pole is first canceled by the compensator zero $s = -k_i/k_p$, and the loop gain assumes the form $\ell(s) = k_p/(Ls)$. Then, the closed-loop transfer function, that is, $\ell(s)/(1 + \ell(s))$, becomes

$$\frac{I_d(s)}{I_{dref}(s)} = G_i(s) = \frac{1}{\tau_i s + 1}, \tag{8.55}$$

if

$$k_p = L/\tau_i, \tag{8.56}$$

$$k_i = (R + r_{on})/\tau_i. \tag{8.57}$$

where τ_i is the time constant of the resultant closed-loop system.

Equation (8.55) indicates that, if k_p and k_i are selected based on (8.56) and (8.57), the response of $i_d(t)$ to $i_{dref}(t)$ is based on a first-order transfer function whose time constant τ_i is a design choice. τ_i should be made small for a fast current-control response but adequately large such that $1/\tau_i$, that is, the bandwidth of the closed-loop control system, is considerably smaller, for example, 10 times, than the switching frequency of the VSC (expressed in rad/s). Depending on the requirements of a specific application and the converter switching frequency, τ_i is typically selected in the range of 0.5–5 ms. The same compensator as $k_d(s)$ can also be adopted for the q-axis compensator $k_q(s)$. Example 8.2 demonstrates the design procedures.

EXAMPLE 8.2 Dynamic Performance of Real-/Reactive-Power Controller

Consider the real-/reactive-power controller of Figure 8.3 with parameters $L = 100$ μH, $R = 0.75$ mΩ, $r_{on} = 0.88$ $m\Omega$, $V_d = 1.0$ V, $V_{DC} = 1250$ V, and $f_s = 3420$ Hz. The AC system frequency and line-to-line rms voltage are $\omega_0 = 377$ rad/s and 480 V (i.e., $V_{sd} = 391$ V), respectively. The transfer function of the feed-forward filter is $G_{ff}(s) = 1/(8 \times 10^{-6}s + 1)$. The PLL of Example 8.1 is used to synchronize the dq-frame to the AC system voltage.

Assuming a closed-loop time constant of $\tau_i = 2.0$ ms, based on (8.56) and (8.57), we deduce the following d- and q-axis compensators:

$$k_d(s) = k_q(s) = \frac{0.05s + 0.815}{s} \quad [\Omega].$$

The system is subjected to the following sequence of events: until $t = 0.15$ s, the gating pulses are blocked and the controllers are inactive. This permits the PLL to reach its steady state. At $t = 0.15$ s, the gating pulses are unblocked and the controllers are activated, while $P_{sref} = Q_{sref} \equiv 0$. At $t = 0.20$ s, P_{sref} is subjected to a step change from 0 to 2.5 MW. At $t = 0.30$ s, P_{sref} is subjected to another step change from 2.5 to −2.5 MW. At $t = 0.35$ s, Q_{sref} is subjected to a step change from 0 to 1.0 MVAr.

Figure 8.12 illustrates the time responses of the VSC system to the start-up process and the disturbances. Figure 8.12 illustrates that P_s and Q_s rapidly track P_{sref} and Q_{sref}, respectively. Figure 8.12 also shows that the responses of P_s and Q_s are decoupled when either of them is changed. Figure 8.12 also illustrates the AC system phase-a voltage waveform, that is, V_{sa}, and the converter phase-a current waveform, that is, i_a. Figure 8.12 shows that i_a is (i) in phase with V_{sa} when $(P_s, Q_s) = (2.5$ MW, 0), (ii) 180° behind V_{sa} when $(P_s, Q_s) = (-2.5$ MW, 0), and (iii) 158° behind V_{sa} when $(P_s, Q_s) = (-2.5$ MW, 1.0 MVAr).

Figure 8.13 provides a close-up of i_d and i_q around $t = 0.20$ s. Figure 8.13 verifies that the step response of i_d is that of a first-order exponential function that reaches its final value at about $t = 0.21$ s, that is, after about 10 ms. It should be noted that such an inspective verification is not readily possible for $\alpha\beta$-frame current controllers of Chapter 7. The reason is that compensators in $\alpha\beta$-frame are essentially of high dynamic orders, and so are the resultant closed-loop

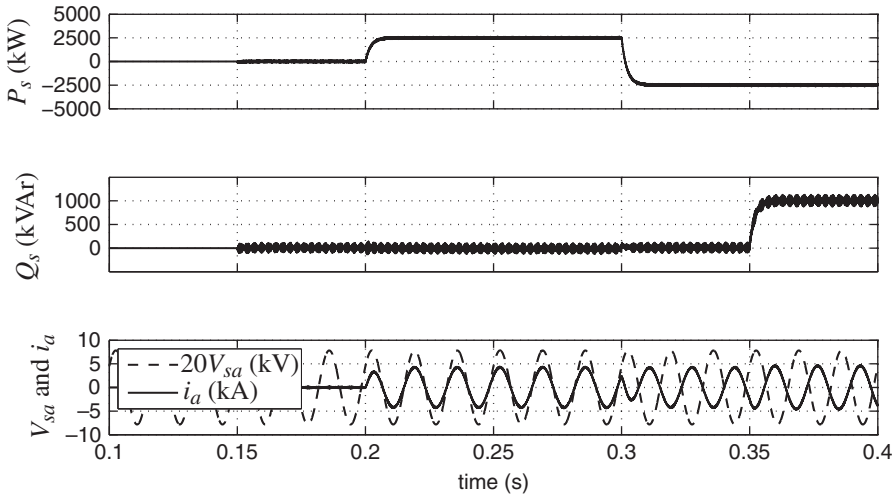

FIGURE 8.12 Dynamic responses of real and reactive power; Example 8.2.

systems. To design $\alpha\beta$-frame compensators, we adopted the frequency response method (Bode plots) that usually does not offer a quantitative insight into the time-response characteristics of the closed-loop system, unless the closed-loop system is predominantly a first-order or a second-order system. Figure 8.13 also confirms that i_d and i_q are well decoupled; it is observed that i_q remains regulated at zero while i_d is changing from zero to 4.26 kA. Ripples on the waveforms of i_d and i_q are due to the pulse-width modulation (PWM) switching side-band harmonics of VSC AC-side currents, which are modulated by 60 Hz via the *abc*- to *dq*-frame transformation.

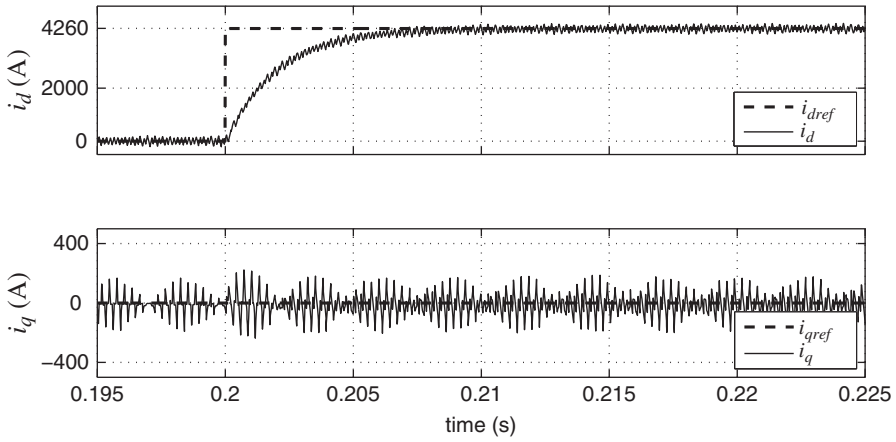

FIGURE 8.13 A close-up of responses of i_d and i_q about $t = 0.20$ s; Example 8.2.

8.4.2 Selection of DC-Bus Voltage Level

As discussed in Sections 7.3.4, 7.3.5, and 7.3.6, the DC-bus voltage of the real-/reactive-power controller of Figure 8.3 must satisfy the following criteria:

$$V_{DC} \geq 2\widehat{V}_t, \quad \text{PWM}, \tag{8.58}$$

$$V_{DC} \geq 1.74\widehat{V}_t, \quad \text{PWM with third-harmonic injection}. \tag{8.59}$$

Thus, one must properly evaluate $\widehat{V}_t$ under the worst-case operating condition. Since the VSC system controls P_s and Q_s, $\widehat{V}_t$ should also be expressed in terms of P_s and Q_s. Based on (8.45) and (8.46), and under the assumptions that $V_{sq} = 0$ and $(R + r_{on}) \approx 0$, we deduce

$$V_{td} = L\frac{di_d}{dt} - L\omega_0 i_q + V_{sd}, \tag{8.60}$$

$$V_{tq} = L\frac{di_q}{dt} + L\omega_0 i_d. \tag{8.61}$$

Substituting for i_d and i_q from (8.41) and (8.42) in (8.60) and (8.61), and assuming that V_{sd} is constant, we obtain

$$V_{td} = \left(\frac{2L}{3V_{sd}}\right)\frac{dP_s}{dt} + \left(\frac{2L\omega_0}{3V_{sd}}\right)Q_s + V_{sd}, \tag{8.62}$$

$$V_{tq} = -\left(\frac{2L}{3V_{sd}}\right)\frac{dQ_s}{dt} + \left(\frac{2L\omega_0}{3V_{sd}}\right)P_s. \tag{8.63}$$

Based on (4.77), the amplitude of the AC-side terminal voltage is

$$\widehat{V}_t = \sqrt{V_{td}^2 + V_{tq}^2}. \tag{8.64}$$

Furthermore, the amplitude of the modulating signal is

$$\widehat{V}_t = \widehat{m}\frac{V_{DC}}{2}. \tag{8.65}$$

As discussed in Section 7.3.6, if the conventional PWM is employed, $\widehat{m}$ can assume a value up to unity, whereas with the PWM with third-harmonic injection, $\widehat{m}$ can be as large as 1.15.

To calculate the maximum of $\widehat{V}_t$, consider the following worst-case scenario. Initially, the system is under a steady-state condition, that is, $P_s = P_{sref} = P_{s0}$ and $Q_s = Q_{sref} = Q_{s0}$. At $t = t_0$, P_{sref} and Q_{sref} are subjected to step changes from P_{s0} to $P_{s0} + \Delta P_s$, and Q_{s0} to $Q_{s0} + \Delta Q_s$, respectively. As discussed in Section 8.4.1,

P_s and Q_s respond to step changes in their corresponding reference commands as

$$P_s(t) = (P_{s0} + \Delta P_s) - \Delta P_s e^{-(t-t_0)/\tau_i}, \tag{8.66}$$

$$Q_s(t) = (Q_{s0} + \Delta Q_s) - \Delta Q_s e^{-(t-t_0)/\tau_i}, \tag{8.67}$$

for $t \geq t_0$. Substituting for $P_s(t)$ and $Q_s(t)$ in (8.62) and (8.63), from (8.66) and (8.67), we deduce

$$V_{td} = V_{sd} + \left(\frac{2L\omega_0}{3V_{sd}}\right)(Q_{s0} + \Delta Q_s) + \left(\frac{2L\omega_0}{3V_{sd}}\right)\left(\frac{\Delta P_s}{\omega_0 \tau_i} - \Delta Q_s\right) e^{-(t-t_0)/\tau_i}, \tag{8.68}$$

$$V_{tq} = \left(\frac{2L\omega_0}{3V_{sd}}\right)(P_{s0} + \Delta P_s) - \left(\frac{2L\omega_0}{3V_{sd}}\right)\left(\frac{\Delta Q_s}{\omega_0 \tau_i} + \Delta P_s\right) e^{-(t-t_0)/\tau_i}. \tag{8.69}$$

Equation (8.68) indicates that at $t = t_0$, V_{td} jumps from the initial value of $V_{sd} + (\frac{2L\omega_0}{3V_{sd}})Q_{s0}$ to $V_{sd} + (\frac{2L\omega_0}{3V_{sd}})Q_{s0} + (\frac{2L}{3\tau_i V_{sd}})\Delta P_s$ and then exponentially approaches the final value of $V_{sd} + (\frac{2L\omega_0}{3V_{sd}})(Q_{s0} + \Delta Q_s)$. Equation (8.69) indicates that V_{tq} jumps from the initial value of $(\frac{2L\omega_0}{3V_{sd}})P_{s0}$ to $(\frac{2L\omega_0}{3V_{sd}})P_{s0} - (\frac{2L}{3\tau_i V_{sd}})\Delta Q_s$ at $t = t_0$ and then exponentially approaches the final value of $(\frac{2L\omega_0}{3V_{sd}})(P_{s0} + \Delta P_s)$. The worst-case scenario corresponds to $t = t_0^+$ (immediately after $t = t_0$) where the jumps in both P_s and Q_s coincide, and

$$V_{td}(t_0^+) = V_{sd} + \left(\frac{2L\omega_0}{3V_{sd}}\right) Q_{s0} + \left(\frac{2L}{3\tau_i V_{sd}}\right) \Delta P_s, \tag{8.70}$$

$$V_{tq}(t_0^+) = \left(\frac{2L\omega_0}{3V_{sd}}\right) P_{s0} - \left(\frac{2L}{3\tau_i V_{sd}}\right) \Delta Q_s. \tag{8.71}$$

Depending on the steady-state power flow and the values of ΔP_s and ΔQ_s, $V_{td}(t_0^+)$ and $V_{tq}(t_0^+)$ can be estimated based on (8.70) and (8.71). The maximum AC-side terminal voltage, $\widehat{V}_t(t_0^+)$, is then calculated from (8.64), based on $V_{td}(t_0^+)$ and $V_{tq}(t_0^+)$. Finally, the minimum required DC-bus voltage is calculated based on (8.58) or (8.59), depending on the PWM strategy adopted. These calculations are demonstrated in Example 8.3.

EXAMPLE 8.3 Selection of DC-Bus Voltage Level

Consider the real-/reactive-power controller of Example 8.2, in which $V_{sd} = 0.391$ kV, $L = 100$ μH, $\tau_i = 2.0$ ms, and $V_{DC} = 1.250$ kV. Assume that for this system the worst-case scenario corresponds to $P_{s0} = 0$, $\Delta P_s = 2.5$ MW, $Q_{s0} = 0$, and $\Delta Q_s = 0$. Thus, based on (8.70), (8.71), and (8.64), $V_{td}(t_0^+) = 0.604$ kV, $V_{tq}(t_0^+) = 0$, and $\widehat{V}_t(t_0^+) = 0.604$ kV. If the conventional sinusoidal

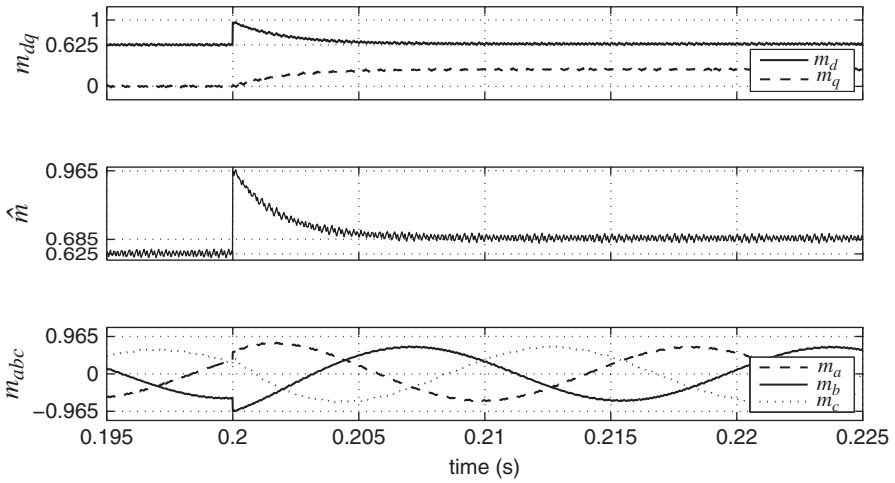

FIGURE 8.14 Steady-state and dynamic responses of the modulating signals to step change in P_{sref}; Example 8.3.

PWM is employed, V_{DC} must be larger than 1.208 kV (equation (8.58)) to avoid overmodulation. However, if the third-harmonic injected PWM is employed, V_{DC} can be lowered to about 1.050 kV (equation (8.59)). For the VSC system of Example 8.2, $V_{DC} = 1.250$ kV was selected since the conventional PWM was employed.

Figure 8.14 illustrates the waveforms of m_d, m_q, and $\widehat{m}$ for the VSC system of Example 8.2. Figure 8.14 illustrates that at $t_0 = 0.2$ s, $\widehat{m}$ jumps to 0.965, corresponding to $\widehat{V}_t = 0.604$ kV. Figure 8.14 also indicates that in this specific example, the instant when the disturbance takes place coincides with the instant when $m_b(t)$ reaches its negative peak; this corresponds to the worst-case scenario. However, since the DC-bus voltage is adequately large, neither $\widehat{m}$ nor $|m_b(t_0)|$ exceed unity, and the VSC does not experience overmodulation.

8.4.3 AC-Side Equivalent Circuit

Traditionally, balanced three-phase linear circuits have been analyzed based on their corresponding phasor diagrams and single-phase equivalent circuits. In the conventional phasor analysis, which is restricted to steady-state conditions, the voltages and currents are represented by phasors, and the passive elements are represented by impedances. This section first presents a space-phasor diagram, analogous to the conventional phasor diagram, for the AC side of the real-/reactive-power controller of Figure 8.3. Then, the relationships between the magnitude/phase-angle of an AC-side variable and the d-/q-axis components of the variable are identified. It is also demonstrated that, under steady-state conditions, the space-phasor differential equations of the real-/reactive-power controller become equivalent to the algebraic

equations derived based on the conventional phasor-domain analysis. Finally, based on the steady-state phasor model, a simplified equivalent circuit is presented for the real-/reactive-power controller of Figure 8.3.

8.4.3.1 Space-Phasor Diagram of the AC Side With reference to the real-/reactive-power controller of Figure 8.3, V_{sabc}, V_{tabc}, and i_{abc} are

$$\begin{aligned} V_{sa}(t) &= \widehat{V}_s \cos(\theta), \\ V_{sb}(t) &= \widehat{V}_s \cos\left(\theta - \frac{2\pi}{3}\right), \\ V_{sc}(t) &= \widehat{V}_s \cos\left(\theta - \frac{4\pi}{3}\right), \end{aligned} \tag{8.72}$$

$$\begin{aligned} V_{ta}(t) &= \widehat{V}_t \cos(\theta + \delta), \\ V_{tb}(t) &= \widehat{V}_t \cos\left(\theta + \delta - \frac{2\pi}{3}\right), \\ V_{tc}(t) &= \widehat{V}_t \cos\left(\theta + \delta - \frac{4\pi}{3}\right), \end{aligned} \tag{8.73}$$

$$\begin{aligned} i_a(t) &= \widehat{i} \cos(\theta - \phi), \\ i_b(t) &= \widehat{i} \cos\left(\theta - \phi - \frac{2\pi}{3}\right), \\ i_c(t) &= \widehat{i} \cos\left(\theta - \phi - \frac{4\pi}{3}\right), \end{aligned} \tag{8.74}$$

where $\theta = \omega_0 t + \theta_0$, and δ and $-\phi$ are the phase shifts of V_{tabc} and i_{abc} with respect to V_{sabc}, respectively. V_{sabc}, V_{tabc}, and i_{abc} are equivalently expressed by the space phasors

$$\overrightarrow{V_s} = \widehat{V}_s e^{j\theta}, \tag{8.75}$$

$$\overrightarrow{V_t} = \left(\widehat{V}_t e^{j\delta}\right) e^{j\theta}, \tag{8.76}$$

$$\overrightarrow{i} = \left(\widehat{i} e^{-j\phi}\right) e^{j\theta}. \tag{8.77}$$

The space phasors $\overrightarrow{V_t}$ and $\overrightarrow{i}$ are phase shifted with respect to $\overrightarrow{V_s}$ by angles δ and $-\phi$, respectively. Under transient conditions, in addition to δ and ϕ, the magnitudes of $\overrightarrow{V_t}$ and $\overrightarrow{i}$ (i.e., $\widehat{V}_t$ and $\widehat{i}$) can also change with time. In a steady state, however,

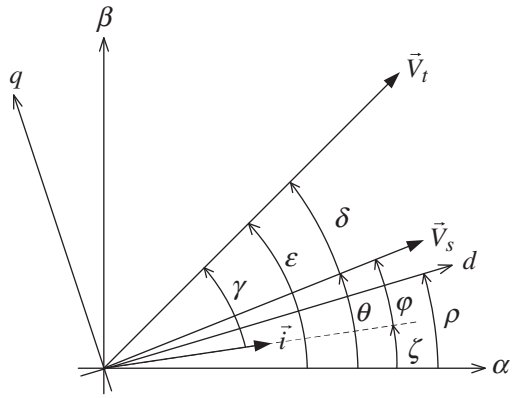

FIGURE 8.15 Space-phasor diagram for AC side of real-/reactive-power controller of Figure 8.3.

δ, ϕ, $\widehat{V}_t$, and $\widehat{i}$ are constant values, and $\overrightarrow{V_s}$, $\overrightarrow{V_t}$, and $\overrightarrow{i}$ assume constant lengths and rotate with the constant angular frequency ω_0.

Figure 8.15 illustrates the space phasors $\overrightarrow{V_s}$, $\overrightarrow{V_t}$, and $\overrightarrow{i}$ on the $\alpha\beta$-plane. Figure 8.15 also shows a dq-frame whose d-axis makes an angle ρ with respect to the α-axis. The d or q component of each space phasor is the projection of the space phasor on the corresponding axis. Therefore, if $d\rho/dt = \omega_0$, that is, the dq-frame rotates with the angular speed ω_0, then V_{sdq}, V_{tdq}, and i_{dq} settle at constant values in steady state. As discussed earlier in this chapter, the PLL not only guarantees $d\rho/dt = \omega_0$ but also ensures that $\rho = \theta$; the latter implies that $V_{sq} = 0$ and $V_{sd} = \widehat{V}_s$, as perceived from Figure 8.15.

To relate the lengths and phase angles of the space phasors to their d- and q-axis components, we use the space-phasor to dq-frame transformation of (8.1), with $\rho = \theta$. This yields

$$V_{sd} + jV_{sq} = \widehat{V}_s, \tag{8.78}$$

$$V_{td} + jV_{tq} = \widehat{V}_t e^{j\delta} = \left(\widehat{V}_t \cos\delta\right) + j\left(\widehat{V}_t \sin\delta\right), \tag{8.79}$$

$$i_d + ji_q = \widehat{i}e^{-j\phi} = \left(\widehat{i}\cos\phi\right) + j\left(-\widehat{i}\sin\phi\right). \tag{8.80}$$

It follows from (8.79) and (8.80) that

$$\delta = \tan^{-1}\left(V_{tq}/V_{td}\right), \tag{8.81}$$

$$\phi = -\tan^{-1}\left(i_q/i_d\right). \tag{8.82}$$

The angles of $\overrightarrow{V_t}$ and $\overrightarrow{i}$ with respect to the α-axis are identified as ε and ζ, respectively. Figure 8.15 illustrates that $\varepsilon = \theta + \delta$ and $\zeta = \theta - \phi$. Thus,

$$\varepsilon = \theta + \tan^{-1}\left(V_{tq}/V_{td}\right), \tag{8.83}$$

$$\zeta = \theta + \tan^{-1}\left(i_q/i_d\right). \tag{8.84}$$

Figure 8.15 also shows that $\gamma = \varepsilon - \zeta$ is the angle of $\overrightarrow{V_t}$ with respect to $\overrightarrow{i}$, that is, γ is the power-factor angle of the three-phase circuit seen from the VSC AC-side terminals. Based on (8.83) and (8.84), we deduce

$$\gamma = \tan^{-1}\left(V_{tq}/V_{td}\right) - \tan^{-1}\left(i_q/i_d\right). \tag{8.85}$$

8.4.3.2 AC-Side Steady-State Equivalent Circuit The AC-side dynamics of the real-/reactive-power controller of Figure 8.3 are described by (8.8). If the PLL is under a steady-state condition, then $\rho = \omega_0 t + \theta_0$ and (8.8) can be rewritten as

$$V_{tdq} - V_{sdq} - L\frac{d}{dt}i_{dq} = \left[jL\omega_0 + (R + r_{on})\right] i_{dq}, \tag{8.86}$$

where $f_{dq} = f_d + jf_q$ and $\omega_0 = d\rho/dt$. In a steady state, the time derivative is zero and we obtain

$$V_{tdq} - V_{sdq} = \underbrace{\left[jL\omega_0 + (R + r_{on})\right]}_{\underline{Z}} i_{dq} = \underline{Z} i_{dq}, \tag{8.87}$$

which is identical to the conventional phasor-domain equation for an equivalent single-phase circuit. Although (8.87) is valid under steady-state conditions, it may also be employed for analysis and control design purposes, if a quasi-steady-state condition is assumed. In this case, i_d and i_q are not constant quantities, but change relatively slowly with time. Therefore, di_d/dt and di_q/dt are insignificant and can be ignored in the analysis.

Figure 8.16(a) illustrates a time-domain equivalent circuit for the AC side of the real-/reactive-power controller of Figure 8.3. Based on (8.86), the circuit of Figure 8.16(a) can be represented by the space-phasor-domain equivalent circuit of Figure 8.16(b). In the circuit of Figure 8.16(b), all the time-domain variables of the original circuit are represented by the corresponding space phasors. Thus, the equivalent circuit is valid under both dynamic and steady-state operating conditions. If a quasi-steady-state condition is assumed, based on (8.87) the circuit of Figure 8.16(a) can be represented by the steady-state phasor-domain circuit of Figure 8.16(c).

Substituting for $\overrightarrow{V_s}$ and $\overrightarrow{i}$, from (8.75) and (8.77), in (4.40), we deduce

$$P_s = \frac{3}{2}\widehat{V}_s\widehat{i}\cos\phi, \tag{8.88}$$

$$Q_s = \frac{3}{2}\widehat{V}_s\widehat{i}\sin\phi. \tag{8.89}$$

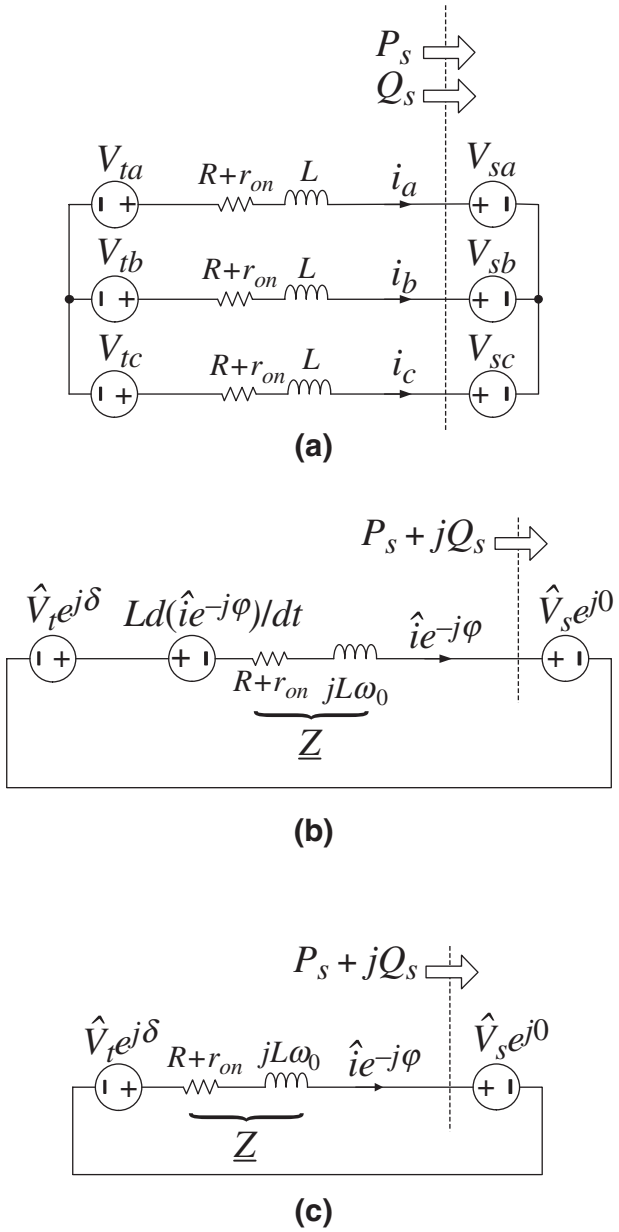

FIGURE 8.16 Equivalent circuits for AC side of the real-/reactive-power controller of Figure 8.3: (a) time-domain equivalent circuit; (b) dynamic space-phasor-domain equivalent circuit; (c) quasi-steady-state space-phasor-domain equivalent circuit.

Equations (8.88) and (8.89) exhibit the same forms as their counterparts in the conventional phasor-domain analysis. However, they are also valid for dynamic operating regimes where $\widehat{V}_s$, $\widehat{i}$, and ϕ can all be functions of time.

8.4.4 PWM with Third-Harmonic Injection

In Section 7.3.6, we explained the need for the third-harmonic injected PWM as a means for extending the VSC permissible voltage range. We then formulated the third-harmonic injected PWM and presented the block diagram of Figure 7.11 for its implementation in $\alpha\beta$-frame. Figure 8.17 shows a block diagram equivalent to that of Figure 7.11, for the third-harmonic injected PWM in dq-frame.

As explained in Section 7.3.6, the modulating signals for the third-harmonic injected PWM are constructed by m_{abc}, based on (7.61)–(7.63). Thus, as shown in Figure 8.17, we obtain m_{abc} from the dq- to abc-frame transformation of m_d and m_q. The third-harmonic injected PWM also requires $\widehat{m}^2$, as indicated by (7.61)–(7.63). Therefore, we express $\widehat{m}^2$ in terms of m_d and m_q as $\widehat{m} = \sqrt{m_d^2 + m_q^2}$ (Fig. 8.17).

Figure 8.18 shows a schematic diagram of a real-/reactive-power controller that employs the third-harmonic injected PWM. The real-/reactive-power controller of

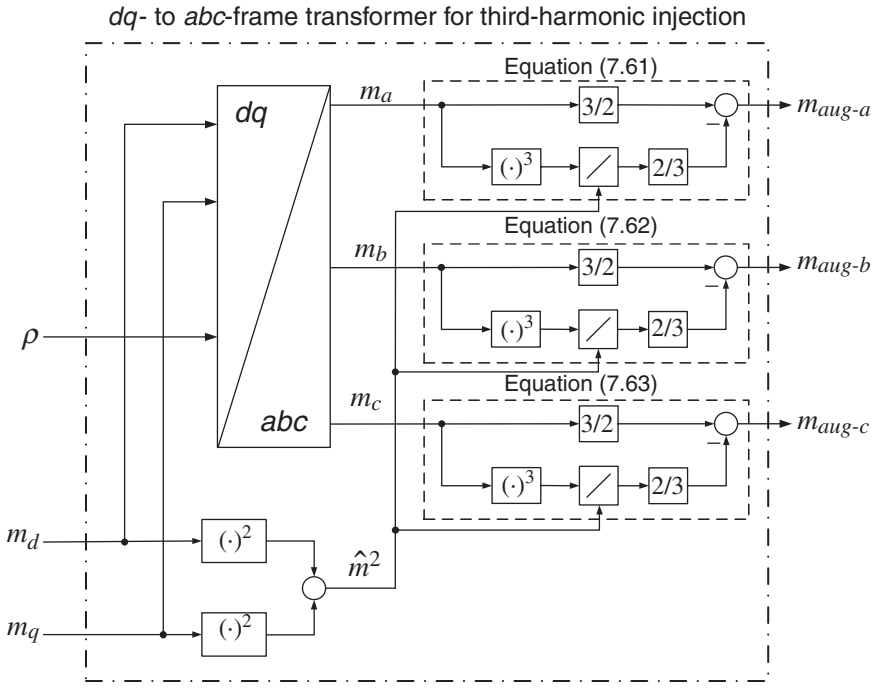

FIGURE 8.17 Block diagram of dq- to abc-frame signal transformer to generate modulating signals for third-harmonic injected PWM.

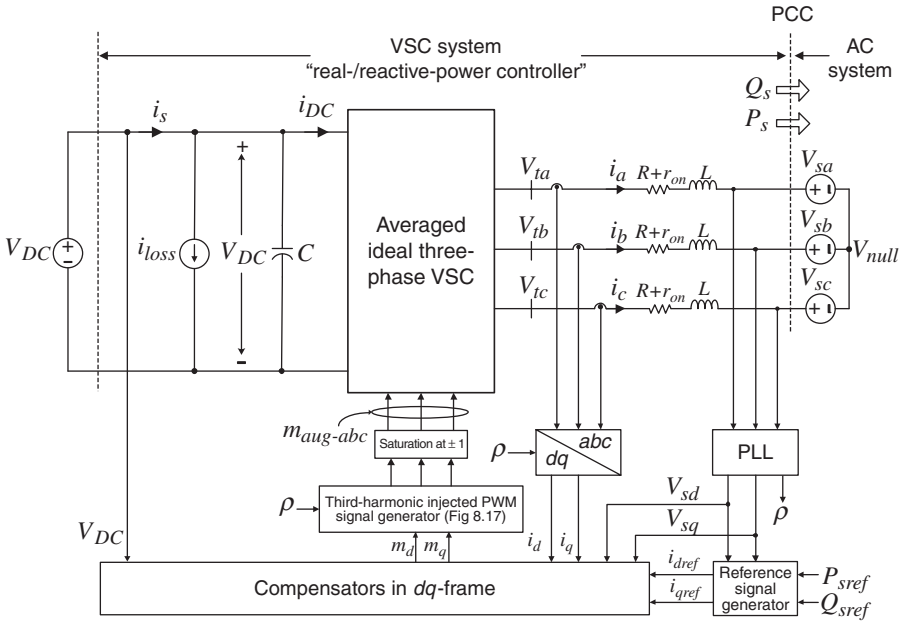

FIGURE 8.18 Schematic diagram of real-/reactive-power controller utilizing the third-harmonic injected PWM.

Figure 8.18 is the same as the real-/reactive-power controller of Figure 8.3 in which the m_{dq}-to-m_{abc} block is replaced by the block diagram of Figure 8.17. The VSC employed in the real-/reactive-power controller of Figure 8.18 can be a two-level VSC or a three-level NPC. Figure 8.18 also illustrates that for the VSC system with the third-harmonic injected PWM, $m_{aug\text{-}abc}$ is limited to ± 1, which corresponds to the limit of ± 1.15 for m_{abc}. Thus, using the third-harmonic injected PWM, the VSC AC-side terminal voltage can reach up to $\pm 1.15(V_{DC}/2)$, instead of $\pm(V_{DC}/2)$ under the conventional PWM.

8.5 REAL-/REACTIVE-POWER CONTROLLER BASED ON THREE-LEVEL NPC

The real-/reactive-power controllers of Figures 8.3 and 8.18 can also utilize the three-level NPC (Fig. 8.19) as the power processor. Based on the unified dynamic model of Section 6.7.4 presented for the two-level VSC and the three-level NPC, the *dq*-frame model and control design procedures presented in Sections 8.3 and 8.4 are equally applicable to both the two-level VSC and the three-level NPC. However, as shown in Figure 8.19, the three-level NPC also requires a DC-side voltage equalizing scheme, as discussed in Section 6.7.2.

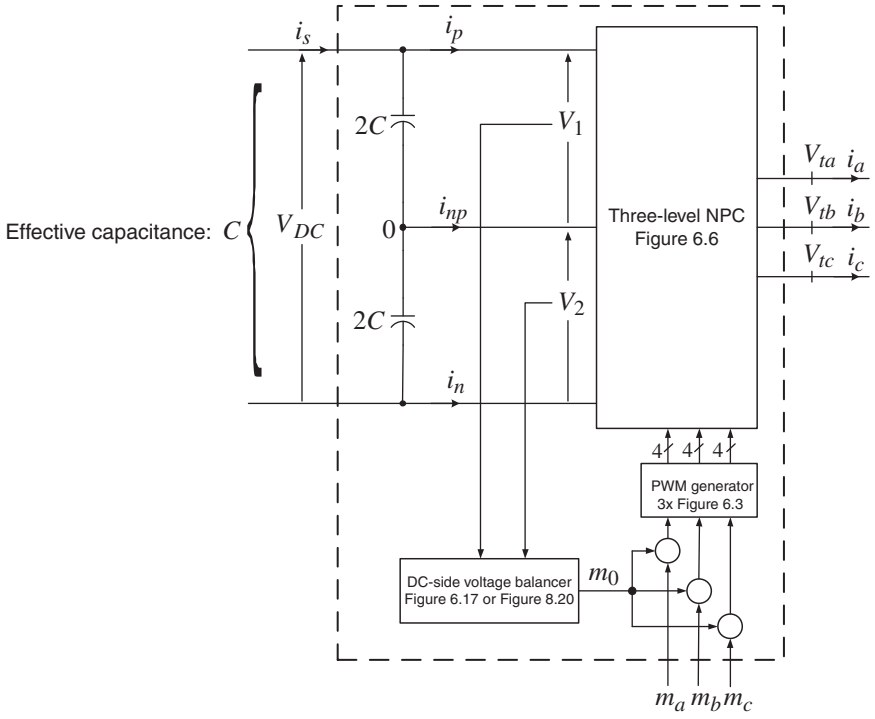

FIGURE 8.19 Block diagram of the three-level NPC.

Figure 8.20 illustrates a control block diagram of the DC-side voltage equalizing scheme. Figure 8.20 indicates that the control plant is an integrator whose gain is proportional to $-P_s$, that is, the real power that the VSC system exchanges with the AC system. Thus, the output of the compensator $K(s)$ is multiplied by -1 if P_s is

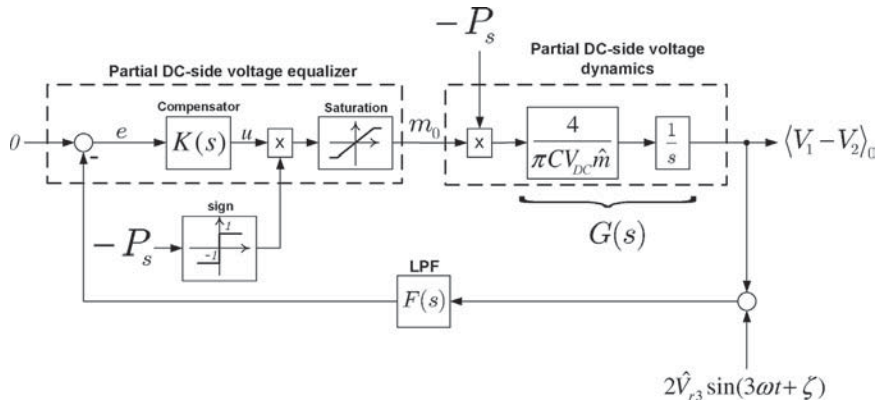

FIGURE 8.20 Control block diagram of the partial DC-side voltage equalizing scheme for the three-level NPC.

positive, to ensure a negative feedback irrespective of the direction of the power flow. P_s can be readily calculated using $P_s = (3/2)V_{sd}i_d$ or, assuming a fast d-axis current controller, approximated by P_{sref}. Figure 8.20 also shows that the difference between the partial DC-side voltages is fed back through a filter, $F(s)$. The filter is required to attenuate the third-order harmonic component of the measured signal and prevent it from distorting the corrective offset m_0. Details of modeling, derivation of the block diagram of Figure 8.20, and the compensator design approach for the DC-side voltage equalizing scheme are given in Section 7.4.

8.6 CONTROLLED DC-VOLTAGE POWER PORT

Previous sections presented the model and controls of the real-/reactive-power controller (Figs. 8.3 and 8.18), whose function is to control the real and reactive power that is exchanged with the AC system. In the real-/reactive-power controller, the VSC DC-bus voltage is impressed by an ideal, DC, voltage source, and the VSC system acts as a bidirectional energy exchanger between the AC system and the DC voltage source. However, in many applications, for example, photovoltaic (PV) systems and fuel-cell systems, the VSC DC side is not interfaced with a voltage source; rather, it is connected to a (DC) power source that needs to be interfaced and exchange (real) power with the AC system. Thus, the DC-bus voltage is not imposed and, therefore, needs to be regulated. This scenario is illustrated in Figure 8.21.

The VSC system of Figure 8.21 is conceptually the same as that of Figure 8.18, except that the DC voltage source is replaced by a (variable) DC power source. The power source typically represents a power-electronic unit (or a cluster of them) with a prime source of energy, for example, a PV array, a variable-speed wind turbine-generator set, a fuel-cell unit, or a gas turbine-generator set, behind it, and is considered as a black box in our investigations. The power source is assumed to exchange a time-varying power, $P_{ext}(t)$, with the VSC DC side. Thus, the VSC system of Figure 8.21 enables a bidirectional power exchange between the power source (black box) and the AC system. We refer to the VSC system of Figure 8.21 as controlled DC-voltage power port, which is employed as an integral part of the STATCOM, the back-to-back HVDC converter system, and variable-speed wind-power units; these are discussed in Chapters 11, 12, and 13, respectively.

The main control objective for the controlled DC-voltage power port is to regulate the DC-bus voltage V_{DC}. As Figure 8.21 illustrates, the kernel of the controlled DC-voltage power port is the real-/reactive-power controller of Figure 8.18 by which P_s and Q_s can be independently controlled. Therefore, to regulate the DC-bus voltage, a feedback mechanism compares V_{DC} with its reference command and accordingly adjusts P_s, such that the net power exchanged with the DC-bus capacitor is kept at zero. However, the reactive power Q_s can be independently controlled. In many applications, Q_s is regulated at zero, that is, the VSC system operates at unity power factor. Alternatively, Q_s may be controlled in a closed-loop mechanism to regulate the PCC voltage, as discussed in Chapter 11.

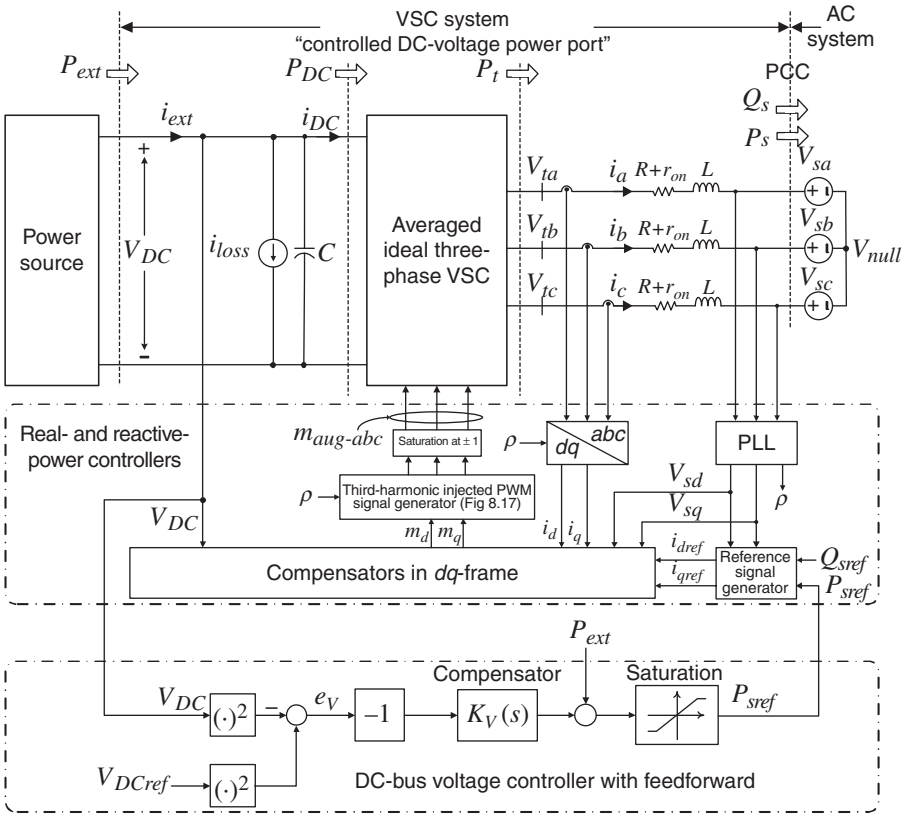

FIGURE 8.21 Schematic diagram of the controlled DC-voltage power-port.

8.6.1 Model of Controlled DC-Voltage Power Port

The main control requirement of the controlled DC-voltage power port of Figure 8.21 is to regulate the DC-bus voltage, V_{DC}. Equivalently, as discussed in Section 7.5.1, we choose to regulate V_{DC}^2 rather than V_{DC}. Based on (7.92), dynamics of V_{DC}^2 are described by

$$\frac{dV_{DC}^2}{dt} = \frac{2}{C}P_{ext} - \frac{2}{C}P_{loss} - \frac{2}{C}\left[P_s + \left(\frac{2LP_s}{3V_{sd}^2}\right)\frac{dP_s}{dt}\right] + \frac{2}{C}\left[\left(\frac{2LQ_s}{3V_{sd}^2}\right)\frac{dQ_s}{dt}\right], \tag{8.90}$$

where $\widehat{V}_s$ of (7.92) is replaced by V_{sd}. Based on the unified dynamic model of the two-level VSC and the three-level NPC that was presented in Section 6.7.4, (8.90) is valid for both VSC configurations. Based on (8.90), V_{DC}^2 is the output, P_s is the

control input, and P_{ext}, P_{loss}, and Q_s are the disturbance inputs. As shown in Figure 8.21, V_{DC}^2 is compared with V_{DCref}^2, the error signal is processed by the compensator $K_v(s)$, and the command P_{sref} is issued for the real-power controller. The real-power controller, in turn, regulates P_s at P_{sref}, while Q_s can be independently controlled. Q_{sref} can be set to a nonzero value if an exchange of reactive power with the AC system is required. In an AC system with a large impedance, the PCC voltage is subject to variations as P_s changes with time (i.e., due to the changes of P_{ext}). In this case, the PCC voltage can be regulated by controlling Q_s in a closed-loop system that feeds the PCC voltage back and commands Q_{sref}; this reactive-power control strategy is discussed in Chapter 11.

To derive the transfer function $G_p(s) = P_s(s)/P_{sref}(s)$, we note that

$$I_d(s) = G_i(s) I_{dref}(s), \tag{8.91}$$

where $G_i(s)$ is given by (8.55). Assuming that V_{sd} is constant, multiplying both sides of (8.91) by $(3/2)V_{sd}$, we obtain

$$P_s(s) = G_i(s) P_{sref}(s). \tag{8.92}$$

Therefore, $G_p(s) = G_i(s)$ and based on (8.55), we have

$$\frac{P_s(s)}{P_{sref}(s)} = G_p(s) = \frac{1}{\tau_i s + 1}. \tag{8.93}$$

The form of (8.93) is intuitively expected as real power in dq-frame is proportional to i_d. The control plant described by (8.90) is nonlinear due to $P_s \frac{dP_s}{dt}$ and $Q_s \frac{dQ_s}{dt}$ terms. The linearized plant is provided by (7.94), which is repeated here as (8.94), in which $\widehat{V}_s$ is substituted by V_{sd}.

$$\begin{aligned} \frac{d\widetilde{V}_{DC}^2}{dt} = \frac{2}{C}\widetilde{P}_{ext} - \frac{2}{C}\left[\widetilde{P}_s + \left(\frac{2LP_{s0}}{3V_{sd}^2}\right)\frac{d\widetilde{P}_s}{dt}\right] \\ + \frac{2}{C}\left[\left(\frac{2LQ_{s0}}{3V_{sd}^2}\right)\frac{d\widetilde{Q}_s}{dt}\right], \end{aligned} \tag{8.94}$$

where superscripts $\sim$ and 0 represent, respectively, small-signal perturbations and steady-state values of the variables. Applying Laplace transform to (8.94), we deduce the transfer function $G_v(s) = \widetilde{V}_{DC}^2/\widetilde{P}_s$ as

$$G_v(s) = \widetilde{V}_{DC}^2(s)/\widetilde{P}_s(s) = -\left(\frac{2}{C}\right)\frac{\tau s + 1}{s}, \tag{8.95}$$

where the time constant τ is

$$\tau = \frac{2LP_{s0}}{3V_{sd}^2} = \frac{2LP_{ext0}}{3V_{sd}^2}. \tag{8.96}$$

Equation (8.96) indicates that τ is proportional to the (steady-state) real-power flow P_{ext0} (or P_{s0}). Thus, if P_{ext0} is small, τ is insignificant and the plant is predominantly an integrator. As P_{ext} increases, τ becomes larger and causes a shift in the phase of $G_v(s)$. In the inverting mode of operation where P_{ext0} is positive, τ is also positive and adds to the phase of $G_v(s)$. However, in the rectifying mode of operation, that is, where P_{ext0} is negative, τ is negative and results in reduction in the phase of $G_v(s)$; the phase drops further as the absolute value of P_{ext0} becomes larger. Based on (8.95), the plant zero is given by $z = -1/\tau$. Therefore, a negative τ corresponds to a zero on the right-half plane (RHP). Consequently, the controlled DC-voltage power port is a non-minimum-phase system in the rectifying mode of operation [72]. As discussed in Section 8.6.3, this non-minimum-phase property has a detrimental impact on the system stability and must be accounted for in the control design process [72].

8.6.2 Control of Controlled DC-Voltage Power Port

Figure 8.22 shows a block diagram of the DC-bus voltage controller for the controlled DC-voltage power port of Figure 8.21. The closed-loop system is composed of the compensator $K_v(s)$, real-power controller $G_p(s)$, and control plant $G_v(s)$, which is described by (8.95). Figures 8.21 and 8.22 indicate that $K_v(s)$ is multiplied by -1 to compensate for the negative sign of $G_v(s)$. The closed-loop system of Figure 8.22 is identical to that of Figure 7.23 for which the design guidelines have been provided in Section 7.5.2 and are, therefore, equally applicable to the closed-loop system of Figure 8.22. As described in Section 7.5.2, $K_v(s)$ should include an integral term and a lead transfer function. The lead transfer function compensates for the plant phase lag and ensures an adequate phase margin at the gain crossover frequency. Based on (8.95) and (8.96), $G_v(s)$ has the largest phase lag when P_{ext} is at its rated negative value. If an adequate phase margin can be guaranteed at this operating point, the closed-loop system remains stable for other operating points.

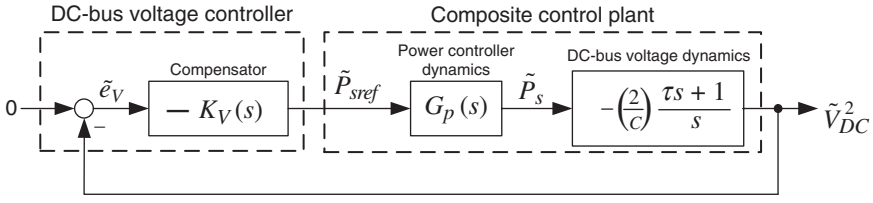

FIGURE 8.22 Control block diagram of DC-bus voltage controller based on the linearized model.

As outlined in Section 7.5.2, to design $K_v(s)$, we first select the gain crossover, ω_c, to be adequately smaller than the bandwidth of $G_p(s)$, such that one can assume $G_p(j\omega_c) \approx 1 + j0$. Then, $K_v(s)$ is designed for an adequately large phase margin under the worst-case operating condition. The design method presented in Section 7.5.2 was based on frequency response. The reason was that based on the $\alpha\beta$-frame control $G_p(s)$ typically is a high-order transfer function and primarily characterized by its bandwidth rather than its pole/zero map. Here, however, $G_p(s)$ (as given by (8.93)) is a first-order transfer function and the root-locus design method is also an option. The advantage of the root-locus method is that performance indices, for example, maximum overshoot and settling time, are related to the pole/zero loci in a more straightforward manner and can be readily taken into account in the design process.

EXAMPLE 8.4 Design of DC-Bus Voltage Controller in *dq*-Frame

Consider the controlled DC-voltage power port of Figure 8.21 that employs the three-level NPC of Figure 8.19. Parameters of the system are $2C = 19{,}250\ \mu\text{F}$, $L = 200\ \mu\text{H}$, $R = 2.38\ \text{m}\Omega$, $r_{on} = 0.88\ \text{m}\Omega$, $V_d = 1.0\ \text{V}$, $V_{DC} = 2500\ \text{V}$, $f_s = 1680\ \text{Hz}$, $V_{sd} = 391\ \text{V}$, and $\omega_0 = 377\ \text{rad/s}$. The rated power of the VSC system is $P_s = \pm 2.5\ \text{MW}$, and the third-harmonic injected PWM strategy is adopted.

With reference to Figure 8.20, the controllers of the DC-side voltage equalizing scheme are

$$K(s) = 0.0007 \quad [V^{-1}],$$
$$F(s) = \frac{s^2 + (3\omega_0)^2}{(s + 3\omega_0)^2} = \frac{s^2 + 1131^2}{s^2 + 2262s + 1131^2}.$$

From (8.56) and (8.57), for $\tau_i = 1.0$ ms parameters of the dq-frame current controllers must be $k_p = 0.2\ \Omega$ and $k_i = 3.26\ \Omega/s$, which correspond to

$$G_p(s) = G_i(s) = \frac{1000}{s + 1000}. \tag{8.97}$$

The DC-bus voltage controller is designed based on the block diagram of Figure 8.22. In Figure 8.22, $G_v(s)$ is a function of the operating point (see equations (8.95) and (8.96)). Therefore, $K_v(s)$ is designed for the worst-case operating point in the rectification mode, corresponding to $P_{ext0} = -2.5$ MW. Equation (8.97) indicates that the bandwidth of $G_p(s)$ is 1000 rad/s. Thus, for the control loop of Figure 8.22, we choose ω_c to be about one-fifth of the bandwidth of $G_p(s)$, that is, 200 rad/s, to avoid excessive phase lag in the loop.

Based on Figure 8.22, the loop gain is

$$\ell(s) = -K_v(s)G_p(s)G_v(s), \tag{8.98}$$

where $G_v(s)$ and $G_p(s)$ are given by (8.95) and (8.97), respectively. To ensure zero steady-state errors, $K_v(s)$ must include an integral term. Let $K_v(s)$ be

$$K_v(s) = N(s)\frac{k_0}{s}, \tag{8.99}$$

where $N(s)$ is a proper transfer function with no zero at $s = 0$, and k_0 is a constant gain. Substituting for $G_v(s)$ and $K_v(s)$ in (8.98), respectively, from (8.95) and (8.99), we obtain

$$\ell(s) = N(s)k_0\left(\frac{2}{C}\right)\frac{\tau s + 1}{s^2\,(0.001s + 1)}. \tag{8.100}$$

If $N(s) = 1$, then $k_0 = 180$ yields $|\ell(j200)| = 1$ and

$$\ell(s) = 37423\frac{\tau s + 1}{s^2\,(0.001s + 1)}. \tag{8.101}$$

We refer to (8.101) as the *uncompensated* loop gain.

Figure 8.23 illustrates the magnitude and phase plots of the uncompensated loop gain, for $P_{ext0} = 2.5$ MW, $P_{ext0} = 0$, and $P_{ext0} = -2.5$ MW. Figure 8.23 shows that the magnitude response of the uncompensated loop gain is similar for all three operating points, and $|\ell(j200)| = 1$. However, $\angle\ell(j200)$ is -168°, -191°, and -215°, corresponding to $P_{ext0} = 2.5$, 0, and -2.5 MW, respectively. Therefore, the closed-loop system is poorly stable for $P_{ext0} = 2.5$ MW, and unstable for $P_{ext0} = 0$ and $P_{ext0} = -2.5$ MW. To ensure a stable closed-loop system for all operating points, we correct $\angle\ell(j200)$ by letting $N(s)$ in (8.100) be the lead filter

$$N(s) = n_0\frac{s + (p/\alpha)}{s + p_1}, \tag{8.102}$$

where p is the filter pole, $\alpha\ (> 1)$ is a real constant, and n_0 is the filter gain. The maximum phase of the filter is given by

$$\delta_m = \sin^{-1}\left(\frac{\alpha - 1}{\alpha + 1}\right), \tag{8.103}$$

which corresponds to the frequency

$$\omega_m = \frac{p}{\sqrt{\alpha}}. \tag{8.104}$$

Thus, if a phase margin of, for example, 45° is desired for $P_{ext} = -2.5$ MW, then $\angle N(j200)$ is required to be 80°. Solving for α, p, and n_0, with $\delta_m = 80^\circ$,

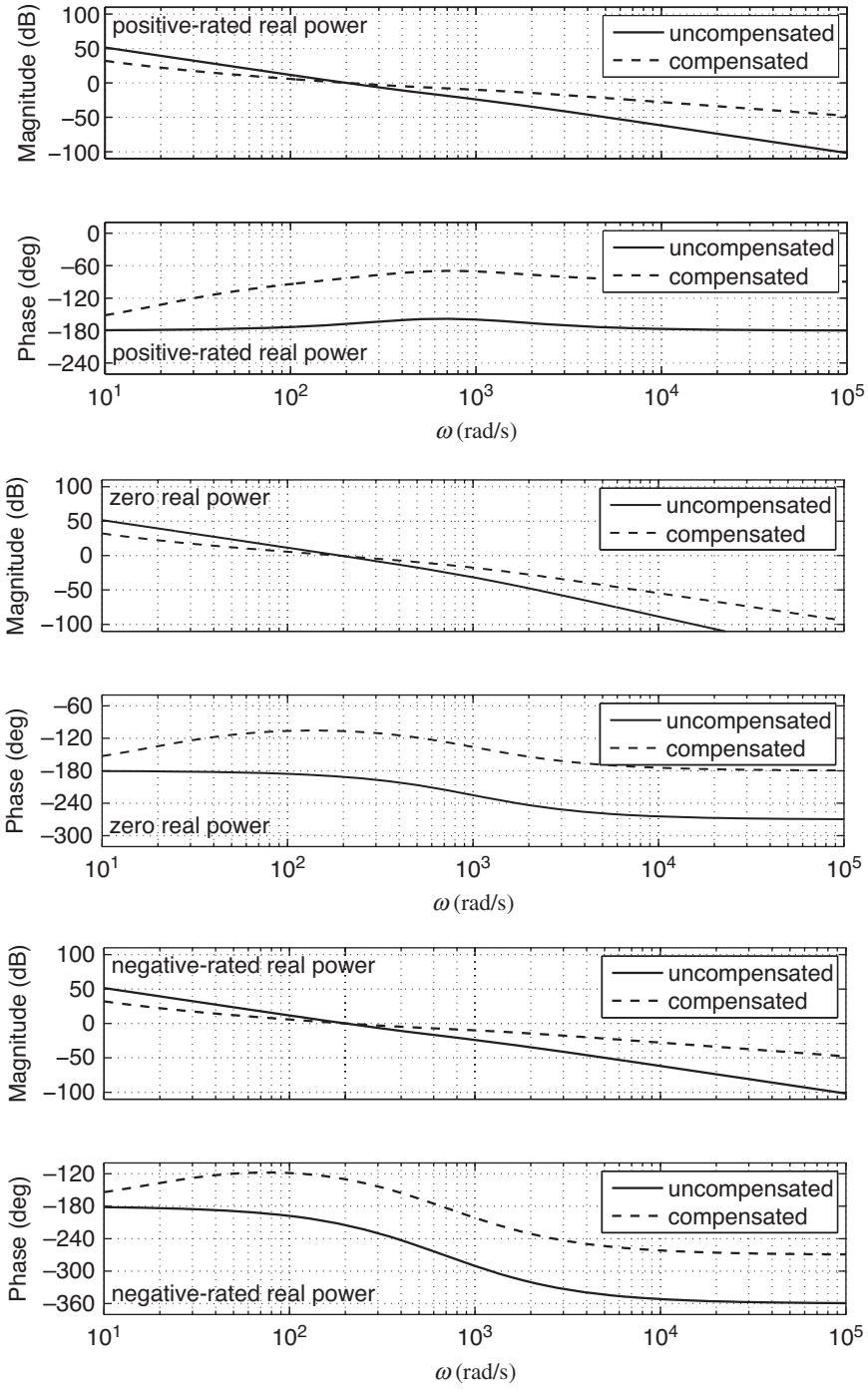

FIGURE 8.23 Bode plot of the open-loop gain of the DC-bus voltage controller; Example 8.4.

$\omega_m = 200$ rad/s, and $|N(j200)| = 1$, we obtain

$$N(s) = 10.38\frac{s+19}{s+2077}. \tag{8.105}$$

Substituting for $N(s)$ in (8.99) and (8.100), from (8.105), we obtain

$$\ell(s) = 388455\left(\frac{s+19}{s+2077}\right)\left(\frac{\tau s+1}{s^2(0.001s+1)}\right), \tag{8.106}$$

$$K_v(s) = 1868\frac{s+19}{s(s+2077)} \quad [\Omega^{-1}]. \tag{8.107}$$

We refer to the loop gain of (8.106) as the *compensated* loop gain. Figure 8.23 also shows the magnitude and phase plots of the compensated loop gain, for $P_{ext0} = 2.5$, 0, and -2.5 MW. Figure 8.23 illustrates that $|\ell(j200)| = 1$ for all three operating points. Moreover, $\angle\ell(j200)$ is -89°, -112°, and -135°, corresponding to $P_{ext0} = 2.5$, 0, and -2.5 MW, respectively. Thus, the closed-loop system is stable for the three operating points with a phase margin ranging from 45° to 91°.

Figure 8.24 illustrates the response of the controlled DC-voltage power port of Figure 8.21 to the start-up process as well as stepwise changes in P_{ext}. The

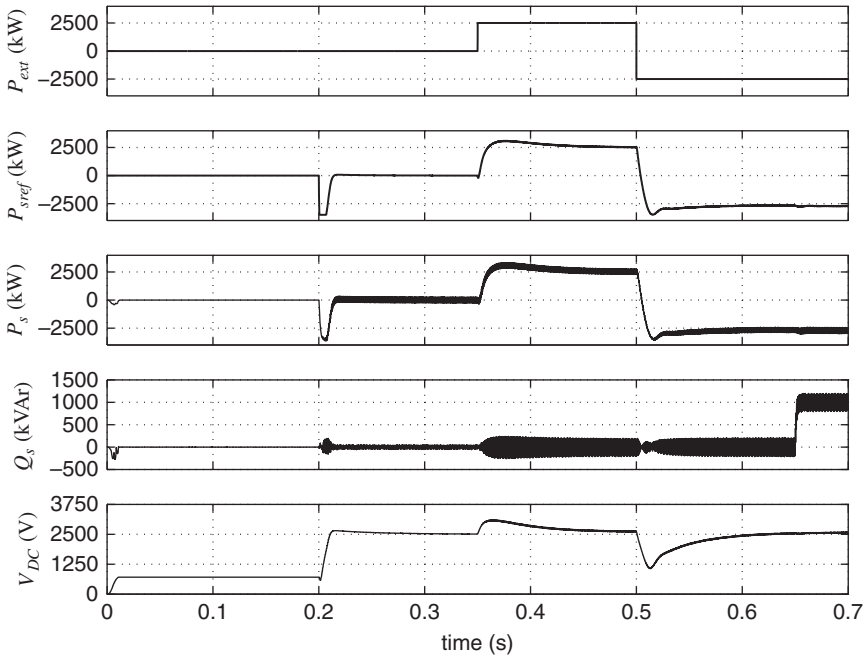

FIGURE 8.24 Dynamic performance of the controlled DC-voltage power port of Example 8.4 when feed-forward compensation is not in service.

results of Figure 8.24 are obtained under the condition that the feed-forward compensation in the DC-bus voltage control loop is disabled, and the VSC system is subjected to the following sequence of events.

Initially, $P_{ext} = 0$, the VSC gating signals are blocked, and the controllers are inactive. However, the DC-side capacitors of the VSC are charged via antiparallel diodes of VSC switch cells, and V_{DC} increases to about 700 V. At $t = 0.20$ s, gating signals are unblocked, all controllers are activated, and V_{DCref} is changed stepwise from 700 to 2500 V. Consequently, to move V_{DC} up, $K_v(s)$ commands a negative P_{sref} to import real power from the AC system to the VSC DC side; P_{sref} is saturated to its negative limit for a brief period. At about $t = 0.30$ s, V_{DC} is regulated at $V_{DCref} = 2500$ V, and P_{sref} and P_s assume small values corresponding to the VSC power loss. Figure 8.24 also shows that P_{ext} changes stepwise from 0 to 2.5 MW, at $t = 0.35$ s, which entails an overshoot in V_{DC}. The compensator reacts to this disturbance and increases P_{sref} (and thus P_s increases) to bring V_{DC} back to 2500 V. At $t = 0.50$ s, P_{ext} changes stepwise from 2.5 to -2.5 MW. Consequently, V_{DC} undergoes an undershoot until the compensator reacts and reduces P_{sref}. It should be noted that the pattern of the undershoot at $t = 0.50$ s is different from that of the overshoot at $t = 0.35$ s. The reason is that, as Figure 8.23 illustrates, the phase margin (and frequency response) is considerably different for these two operating points. Therefore, the system response to disturbances is also different for the two operating points. At $t = 0.65$ s, Q_{sref} assumes a step change from 0 to 1.0 MVAr. This disturbance, however, has no significant impact on V_{DC}, as Figure 8.24 illustrates. The reason is that, based on (8.90), the contribution of Q_s to dV_{DC}^2/dt is weighted by the term $2L/(3V_{sd}^2)$, which typically is a small value.

Figure 8.25 illustrates the response of the controlled DC-voltage power port of Figure 8.21 to the same disturbances as described above, but with the feed-forward compensation of the DC-bus voltage control loop enabled (i.e., a measure of P_{ext} is added to the output of $K_v(s)$, Fig. 8.21). A comparison between Figures 8.25 and 8.24 indicates that deviations of V_{DC} from V_{DCref} are considerably smaller when the feed-forward compensation is employed. The reason is that any change in P_{ext} is rapidly communicated to P_{sref}, and the balance of power is quickly regained.

8.6.3 Simplified and Accurate Models

The DC-bus voltage dynamics, described by (8.90), are nonlinear; the nonlinearity is due to the presence of the instantaneous power of VSC interface reactors. Thus, in the linearized model of (8.95), the time constant τ is a function of the operating point. Based on (8.96), τ is negative in the rectifying mode of operation and results in excessive phase lag in the loop gain. This phase lag can lead to unsatisfactory performance or even instabilities if it is not taken into account in the compensator design.

In the technical literature, the instantaneous power of the interface reactors is often ignored [73–76], that is, it is assumed that $L \approx 0$ and $P_t = P_s$. We refer to this model

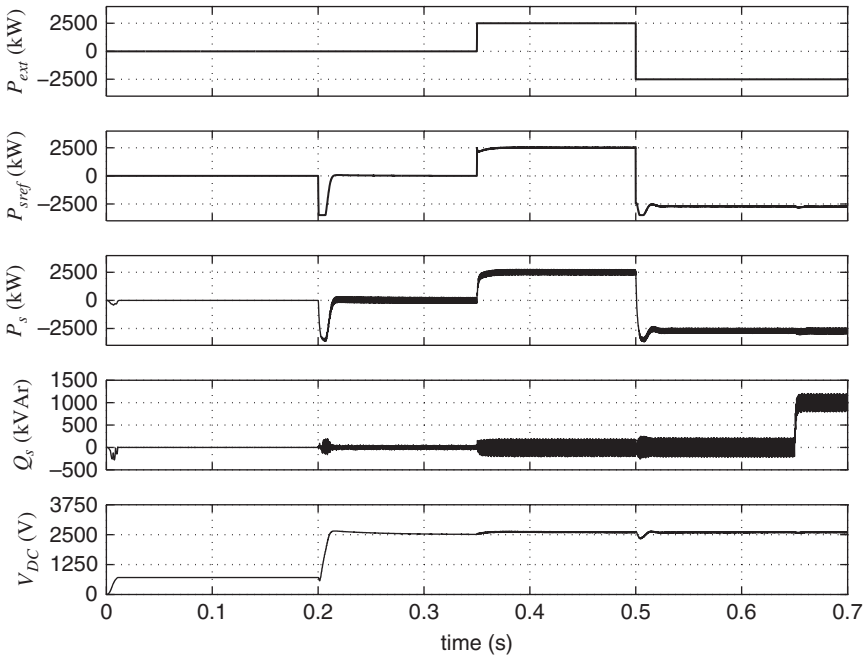

FIGURE 8.25 Dynamic performance of the controlled DC-voltage power port of Example 8.4 when feed-forward compensation is enabled.

as the *simplified model*, which can then be derived from (8.95) by substituting for $\tau = 0$.

$$G_v(s) = V_{DC}^2(s)/P_s(s) = -\left(\frac{2}{C}\right)\frac{1}{s}. \tag{8.108}$$

The transfer function (8.108) indicates that the simplified model corresponds to the accurate model of (8.95) for the zero real-power operating point, that is, $P_{ext0} = 0$. However, as demonstrated in Example 8.4, the zero real-power operating point does not correspond to the worst-case scenario in terms of the compensator design, since the loop gain phase continues to drop in the rectifying mode of operation. Consequently, compensator design based on the simplified model of (8.108) may result in poor performance or even instabilities [72]. This is further highlighted in Example 8.5.

EXAMPLE 8.5 Instability in Rectifying Mode of Operation

Consider the controlled DC-voltage power port of Example 8.4 for which $G_p(s)$ is given by (8.97). Assume that we have to design a PI compensator, for the closed-loop system of Figure 8.22, based on the simplified model of (8.108). Thus, the loop gain includes a double integrator and a negative real pole (i.e.,

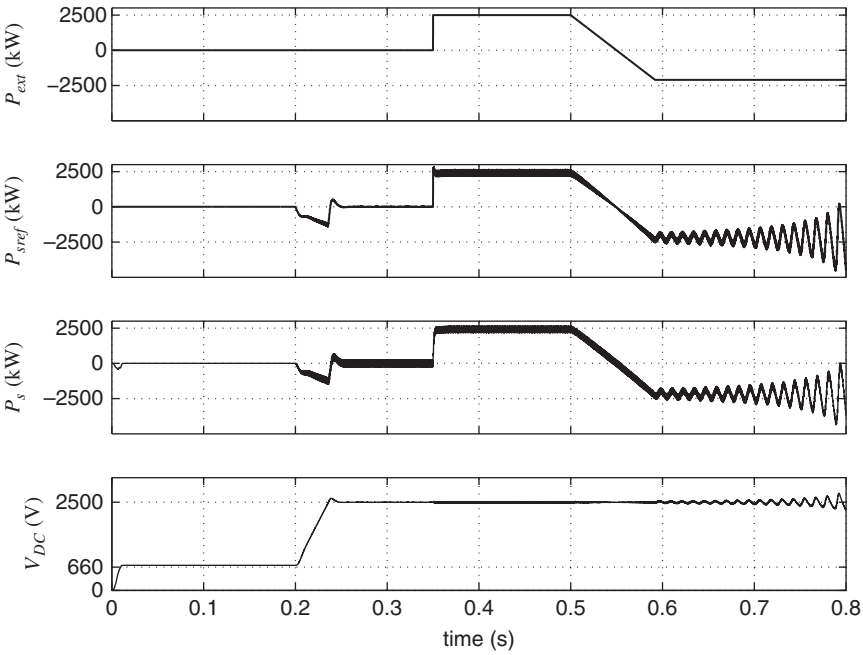

FIGURE 8.26 Instability of the DC-bus voltage controller in the rectifying mode of operation; Example 8.5.

the pole of $G_p(s)$); the compensator design process requires to identify the zero and the gain of the PI compensator. For a loop gain that possesses two integrators (including that of the PI compensator) and one first-order lag, the method of *symmetrical optimum* can be effectively employed to determine the compensator zero [43]. Based on the symmetrical optimum method, one obtains the following compensator that yields a phase margin of 45° and a crossover frequency of $\omega_c = 415$ rad/s:

$$K_v(s) = 1.996\frac{s + 172}{s} \quad [\Omega^{-1}]. \tag{8.109}$$

Since the simplified model of (8.108) does not exhibit any dependence on the operating point, one would expect that the closed-loop system remains stable over the entire power range. This is, however, not the case. Figure 8.26 illustrates that while the closed-loop system is stable for $P_{ext} = 2.5$ MW, it becomes oscillatory and unstable when P_{ext} drops from 2.5 to about -2.1 MW. The reason is that the actual control plant, described by (8.95) rather than (8.108), exhibits a non-minimum-phase zero when P_{ext} becomes negative. For this example, two of the three closed-loop poles lie on the RHP when P_{ext} becomes smaller than about -2.1 MW. These two poles are $s = 4.42 \pm j535$ rad/s and correspond to the observed unstable oscillatory response.

9 Controlled-Frequency VSC System

9.1 INTRODUCTION

Chapters 7 and 8 discussed control and operation of the grid-imposed frequency VSC system in which the operating frequency was predetermined and imposed by the AC system. These chapters implicitly translated the control of the grid-imposed frequency VSC system into the control of real and reactive power that the VSC system exchanges with the AC system, through a current-mode control strategy. This chapter investigates a class of VSC systems in which the operating frequency is not imposed by the AC system, but it is controlled by the VSC system itself. We refer to this class as *controlled-frequency VSC system*, in which the voltage and frequency at the point of common coupling (PCC) are controlled; thus, the real and reactive power that the VSC system exchanges with the AC system are the by-products.

Typical scenarios where a controlled-frequency VSC system is encountered include

- an electronically coupled distributed generation (DG) or distributed energy storage (DES) unit[1] that supplies a dedicated load, or a cluster of loads, under an islanded (off-grid) condition;
- a VSC-based HVDC converter system that supplies a passive or weak AC system; and
- an uninterruptible power supply (UPS) system that adopts a VSC system as its kernel to regulate the frequency and voltage of a sensitive load, for example, under emergency conditions.

In this chapter, we first present a *dq*-frame model for the controlled-frequency VSC system and then introduce a control strategy that does not require prior knowledge of the load model. We achieve this objective through a feed-forward compensation technique that can effectively decouple the VSC system dynamics from those of the load. Finally, we investigate transitions of the VSC system from the controlled-frequency mode to the grid-imposed frequency mode, and vice versa.

[1] These are collectively referred to as distributed energy resource (DER) units.

Voltage-Sourced Converters in Power Systems, by Amirnaser Yazdani and Reza Iravani